Design of Area Efficient Fault Tolerant Full Adder/ Subtractor Using Reversible Logic

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Abstract: Reversible logic is now-a-days emerging as an important research area over conventional logic. It is having variety of applications in fields of Digital Signal Processing, Quantum Computing and Low Power CMOS Design. Irreversible logic gates dissipate power for each bit of data that is lost. It is not likely to consider quantum calculations without execution of reversible logic. The most important purposes of designing reversible logic are to decrease quantum cost, intensity of the circuits and the number of garbage outputs. This paper presents the Full adder/subtractor that uses half adder/subtractor with minimum constant inputs and lesser garbage outputs. Thus the proposed architecture Full Adder/Subtractor is having less number of Constant Inputs and Garbage Outputs than the Existing architecture.

Keywords: Parallel Adder/Subtractor, Reversible logic gates, full-adder, fault-tolerant, reversible computing

I. INTRODUCTION

Irreversible hardware calculation results in power dissipation because of records loss. As per R. Landauer’s studies in the early 1960s, the amount of power (heat) dissipated for each irreversible bit operation is given via KTln2, where K = 1.3806505*10^-23JK^-1 is the Boltzmann constant and 000T is the working temperature [1]. Thus, reversible logic gates (or circuits) are records-lossless. Furthermore, reversible gates are of essential interest in optical computing, low strength design, quantum computing and nanotechnology based totally systems. It isn’t feasible to understand quantum computing without reversible logic.

Neither feedback (loop) nor fan-out is authorized in reversible logic circuits. Thus, synthesis of reversible common sense is different from conventional common sense synthesis [8]. It is more challenging to build a fault-tolerant reversible circuit than a standard logic circuit. The reversible circuits are the ones in which reversible good judgment gates are primary constructing blocks and there may be no power loss. The reversible good judgment gates may be having n-input and n-output i.e. Equal quantity of enter and equal number of output, and additionally with one to-one mapping i.e. Inputs may be uniquely recovered from the outputs.

II. REVERSIBLE LOGIC GATES

The reversible logic gates will produces distinctive output vector form unique input vector or vice-versa [3]. The Fig. 1 shows generally reversible gate will be having k inputs and k outputs, and it is referred to as ok*k reversible gate [4]. In reversible gates fan out are not authorized, if there it ought to now not exceed a couple of. No remarks paths are allowed i.e. Circuit is acyclic. Some important elements are Garbage output, consistent enter and so on. Garbage output is the unutilized output from the reversible gate, very a great deal crucial to obtain reversibility and it must be no longer used for in addition computation. Constant inputs are the ones so one can be introduced to okay*ok characteristic to make it reversible. For an optimized reversible circuit, of rubbish outputs, the number of constant inputs and the quantity of reversible gates used ought to be a minimum.
There exist several reversible gates; some of the basic reversible gates are 2*2 Feynman [5] gate, Peres gate [6] and Toffoli [7, 8] gate etc.

Fault tolerance is the characteristic that will enable the system to prolong its operation properly when a failure occurs in any of the components. If the system is made up, using fault-tolerant components, then the error detection and correction process will be much easier. In communication and other systems fault tolerance is achieved by parity. Parity checking is most widely used method for error detection in digital logic circuits. It will most commonly used in arithmetic and other processing systems because those systems do not store the parity of the data, there have been attempts at performing arithmetic successions on specially encoded operands in a manner to check the parity. These types of methods will require more development and they are not widely used. B.Parhami [9] shown some methods of error detection in reversible circuits, those standard methods of error detection will present some problems because in reversible logic circuits fan out are not permitted, and we have to take care of garbage bits. For parity preserving output data, the data can be checked in manner i.e. For a 3*3 reversible gate it will satisfies the condition of $A \oplus B \oplus C = P \oplus Q \oplus R$, where $A \oplus B \oplus C$ is input parity and $P \oplus Q \oplus R$ is output parity. This means that the gate will be parity preserving.
III. PROPOSED WORK

We have studied adder design using reversible gates by several authors. Some authors are demonstrated that a reversible adder circuit can be realized with as a minimum two rubbish output and one regular enter. For designing fault-tolerant adder circuits, these limitations aren’t suitable because in fault-tolerant circuits the input parity must meet with the output parity. In the beneath segment first we talk fault tolerant half of adder/subtractor layout [12] and after that fault-tolerant complete adder/subtractor design [12] because the full layout adder calls for half adder circuit. This fault-tolerant full adder/subtractor block can used to understand different arithmetic circuits which include ripple convey adder, bring appearance in advance adder, deliver pass good judgment and multiplier/divisors. This paper also proposes the design of a parallel adder/subtractor design.

As per conventional approach for designing reversible full adder it requires two half adders. So the fault tolerant reversible full adder/subtractor (FT_FA/S) circuit is built using two faults tolerant half adder/subtractor (FT_HA/S) channels. The shortcoming tolerant Full Adder/subtractor is acknowledged utilizing Two Modified IG (MIG) door, two Fredkin entryway (FRG) and one Feynman two fold door (F2G) has seemed in Fig. 3. The circuit will be having three inputs A, B & Cin (For full subtractor A, B & Bin are inputs) and a control line ctrl which will controls mode of operation, i.e. At the point when ctrl is at logic 0, the circuit will go about as full snake, and when ctrl is at logic 1 the circuit will go about as full subtractor.

The Fig 5 represents the Fault Tolerant Full Adder/Subtractor (FT_FA/S) circuit with 5 constant inputs are forced at logic 0 and 7 garbage bits g1 to g7.
IV. RESULTS

Fig 6: Simulation result of the 16-bit fault-tolerant ripple carry adder

Fig 7: Block diagram of the 16-bit fault-tolerant ripple carry adder

Fig 8: RTL schematic of the 16-bit fault-tolerant ripple carry adder

Fig 9: Technology schematic of the 16-bit fault-tolerant ripple carry adder

Fig 10: Summary report of the 16-bit fault-tolerant ripple carry adder
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VI. REFERENCES


