Electrical Characteristics of Double Gate and Trigate Silicon-On-Insulator Fin FET based Inverter at 20nm Technology

Jashanjot Kaur
M.Tech Student
Guru Nanak Dev Engineering College, Ludhiana, Punjab, India

Sandeep Singh Gill
Professor
Guru Nanak Dev Engineering College, Ludhiana, Punjab, India

Gurpurneet Kaur
Assistant Professor
Guru Nanak Dev Engineering College, Ludhiana, Punjab, India

Abstract

Due to alarming short channel effects, scaling of the singlegate bulk MOSFETs encounters great challenges in nanometer regime.Therefore Multi-gate FinFETs provides alternative as they have superiorshort channel effects (SCEs) performance compared to the conventional CMOS. In this paper, Doublegate and Trigate SOI p-type FinFETs and n-type FinFETs have been designed for 20nm gate lengthand analyzed in terms of charactersistic parameters. Further FinFETs based invertersusing both Trigate and Doube gate have been implemented and analyzed in terms of noise margin and propagation delay.

Keywords: *Double gate (DG), FinFET, SOI (Silicon-on-Insulator), Subthreshold Swing (SS), TCAD (Technology Computer Aided Design).*

INTRODUCTION

Over the past few decades, the technology is intended on the way to miniaturization of electronic components and transistors in integrated circuits (ICs). Gordon Moore in 1965 prognosticated that in every two years the number of transistors in a chip doubles, however, the reduction in the transistor dimension isobstructed by the SCEs. Beyond 16 nm technology, the CMOS technology can be implemented with the invention of multi-gate transistors like FinFET and is considered to be the best candidate to support the subsequent International Technology Roadmap for Semiconductors (ITRS) scaling trends.Due to the rising need for higher drive current and better short-channel characteristicsin nanometer region, three-dimensional SOI(silicon-on-insulator) devices with multiple gates (double, triple, gate all around etc) are generated from classical, planar, single-gate devices[1].Multi-gate devices are promising structures in case of reduced short channel effects (SCEs), higher current drivability, closely ideal sub-threshold swing (SS), Drain induced barrier lowering(DIBL) and mobility improvement[2], [3].The gate oxide layer in DG FinFET is broad at the top portion of fin as compared to the Trigate FinFETso that only two gates stay effectual for the channel control.The channel width for a FinFET device is given by equation (1),

$$W=2H_{fin} + W_{fin} \quad (1)$$

The widely known basis for restricting SCEs in FinFET devices is association amid the gate length (L_g) and fin width (W_{fin}) which is expressed asL_g= 1.5 * W_{fin}. Currently SOI is the most effective method for increasing the device performance as it decreases the parasitic capacitances of source and drain and has less leakage currents. Also doping of bulk FinFET is complicated as compared to SOI [4].Inverter, NAND and NOR circuits are one of the essential parts of digital system.Inverter is an important circuit device that provides quick transition time, high buffer margins, and low power dissipation.

DEVICE DESIGN AND METHODOLOGY

To investigate the characteristics of Multi-gate SOI FinFET, simulations of designed devices are done using VisualTCAD software. TCAD is a software tool that models semiconductor fabrications and also semiconductor device operation. FinFETs havebeen fabricated on SOI (silicon-on-insulator) wafer. N-type FinFETs and P-type FinFETs using both Double gate and Trigatetechnology have been

designed. Table 1 shows the dimensions used for n-type and p-type FinFET regions and indicates doping value of source, drain and channel. Dimensions are kept same for both Double gate and Trigate Fin FETs; the only difference is in number of gates covering the channel. The work function of the gate electrode is4.75eV and 5.50eV for n-type and p-type FinFETs respectively. Table 2shows material used for various regions. The Buried oxide thickness is kept as 10 nm for all devices. Figure 1 shows DG SOI FinFET. Figure 2 shows Double gate FinFET based Inverter. Figure 3 shows Trigate SOI FinFET. Further inverter has been implemented using the N and P-type Trigate FinFETs as shown in Figure 4.

TABLE 1: Dimensions for FinFETs

Device Parameters	**Dimensions for both DG and Trigate**	
	N-type FinFET	**P-type FinFET**
Gate/ Channel length (L_g, nm)	20	20
Source/ Drain length (L_s/L_d, nm)	17	17
Fin Width (nm)	8	16
Equivalent Oxide Thickness (T_{ox}, nm)	1	1
Channel Doping (N_c, cm^{-3})	2E16	1E20
Source/Drain Doping (N_s/N_d, cm^{-3})	1E20	2E16
Substrate Doping (cm^{-3})	1E15	1E15

TABLE 2: Materials for different regions of FinFET

Region	**Material**	**Type**
Gate	Poly Silicon (NPolySi and PPolySi)	Conductor
Gate Oxide	Hafnium Oxide (HfO_2)	Insulator
Substrate	Silicon (Si)	Semiconductor
Source/Drain (Contact)	Aluminium (Al)	Conductor

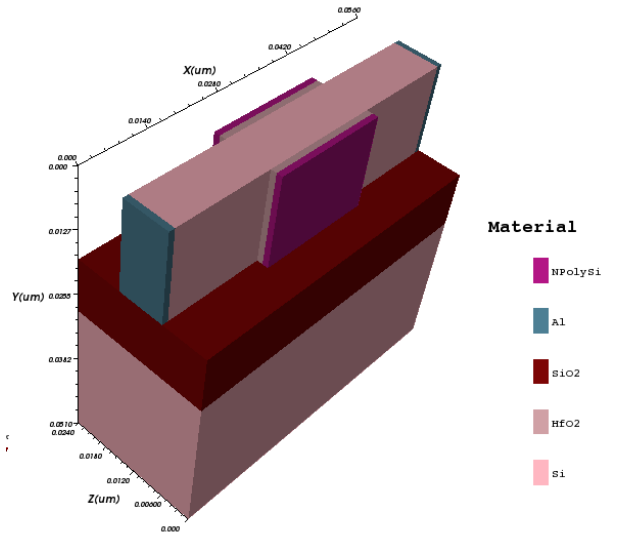

Figure 1: DG SOI FinFET

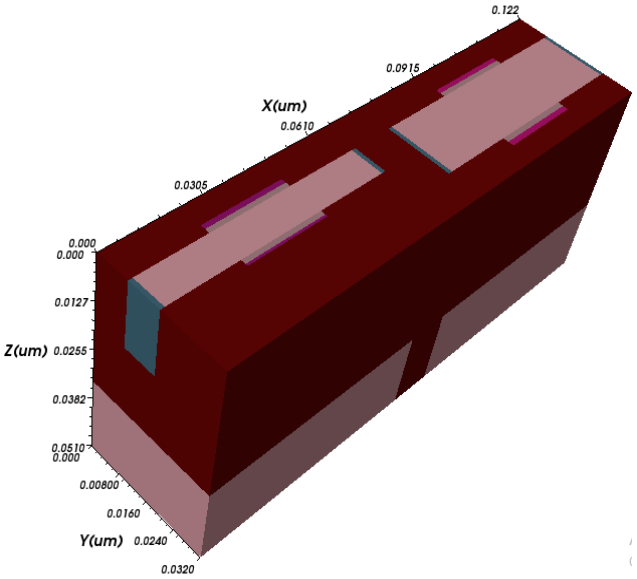

Figure 2: DG FinFETs based Inverter

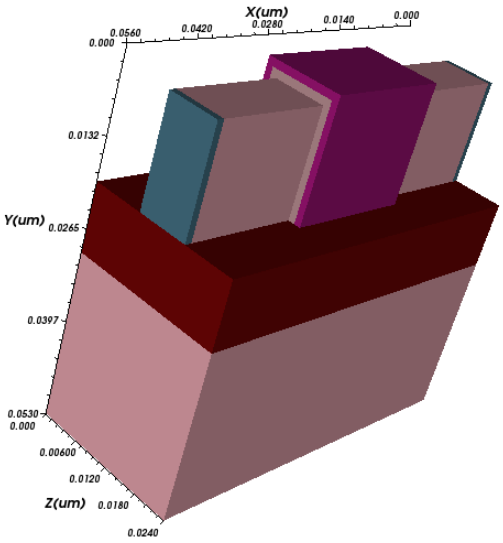

Figure 3: Trigate SOI FinFET

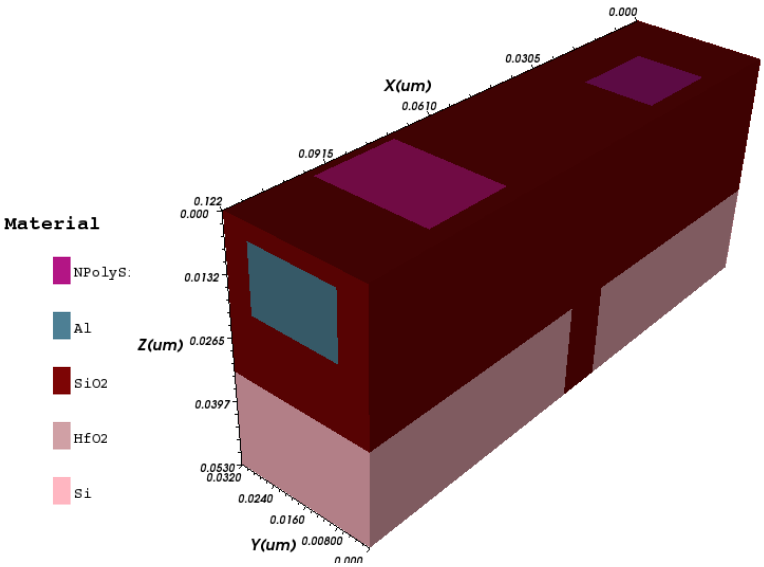

Figure 4: Trigate FinFETs based Inverter

RESULTS AND DISCUSSION

Above designed devices are simulated using Lombardi Mobility Model [5]. The output characteristics of FinFET devices have been obtained with varying drain voltage (0-1.0V) at constant gate voltage V_{gs} = 0.05V. The transfer characteristics have been obtained with varying gate voltage (0-1.0V) at

constant drain voltage V_{ds}= 0.05V. SS is the gate voltage required to alter drain current per decade and is calculated from transfer characteristics.

$$SS = dV_{gs} / d\log (I_d) \qquad (2)$$

From transfer characteristics, at constant drain voltage V_{ds} = 0.05V, on current is taken at V_{gs} = 1.0V and off current is taken at V_{gs} = 0.0V. DIBL is calculated from horizontal displacement of V –I curvefor V_{ds}= 0.02V and 1V. Table 3 indicates the parameters calculated using the V-I characteristics for p-type FETs and Table 4 indicates the parameters calculated for n-type FETs.Figure 5 and Figure 6 shows the Vgs vs Id curves for both DG and trigate n-type FinFETs and p-type FinFETs.

TABLE 3: FinFET parameters and their values

Parameters	**P-type FinFET**	
	DG	**TG**
I_{on} Current (A)	2.060e-05	2.27e-05
I_{off}Current (A)	6.782e-13	4.143e-13
I_{on}/I_{off}	0.304e+8	0.547e+8
SS (mV/dec)	97	71

TABLE 4: FinFET parameters and their values

Parameters	**N-type FinFET**	
	DG	**TG**
I_{on} Current (A)	1.935e-05	1.751e-05
I_{off}Current (A)	6.745e-11	9.644e-12
I_{on}/I_{off}	3.485e+6	0.182e+7
SS (mV/dec)	74	71
DIBL (mV/V)	70	30
Transconductance (S)	7.7e-05	7.83e-05
Transconductance Generation Factor(V^{-1})	27.37	27.51

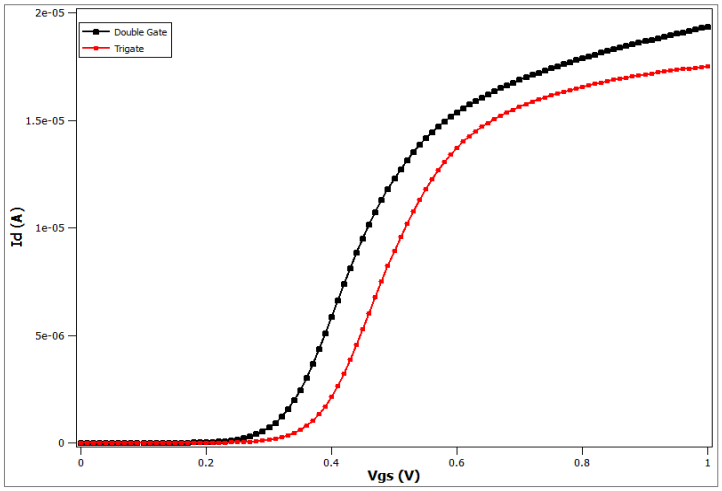

Figure 5: Transfer characteristics for n-type FETs

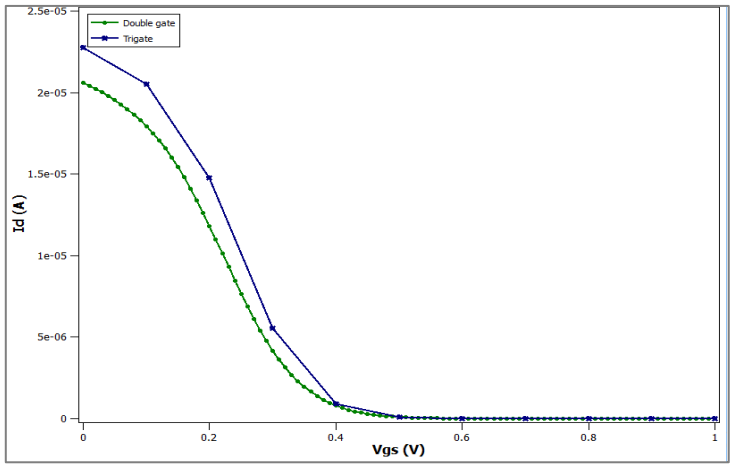

Figure 6: Transfer characteristics for p-type FETs

Figure 7 and Figure 8 shows theVdsvs Id curves for both DG and trigate n-type FinFETs and p-type FinFETs.

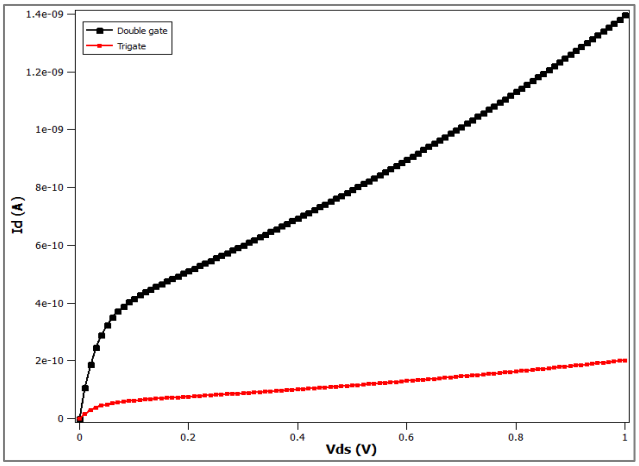

Figure 7: Output characteristics for n-type FETs

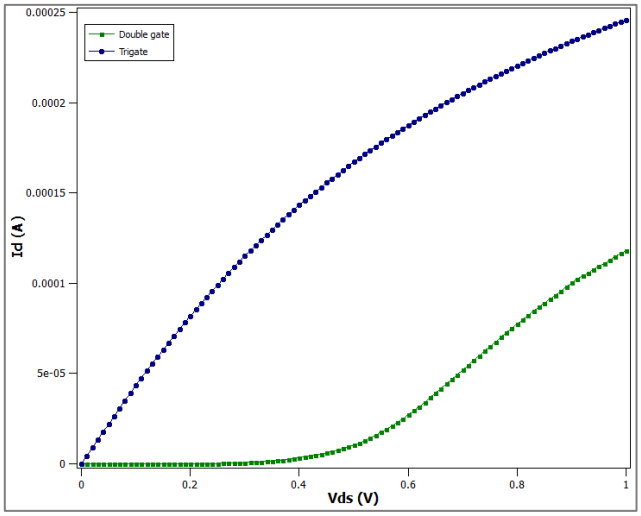

Figure 8: Output characteristics for p-type FETs

Figure 9 shows the transconductance curves for n-type DG and trigate FinFETs. Figure 10 and Figure 11 shows the simulation waveforms for Inverters. Using these waveforms propagation delay is calculated. Propagation delay gives the speed of the inverter. It specifies how rapid the gate responds to variation in input signal. Noise margin implies the ability of inverter to tolerate the noise without affecting the operation of inverter circuit. It guarantees that if disturbances within the range of calculated noise margin interferes with the input signal then the signal remains unchanged i.e., logic 1 will remain as logic 1 and not switches to logic 0 and vice versa [6]. Table 5 shows the parameters (propagation delay and noise margin) calculated for DG and trigate FinFETs based inverters.

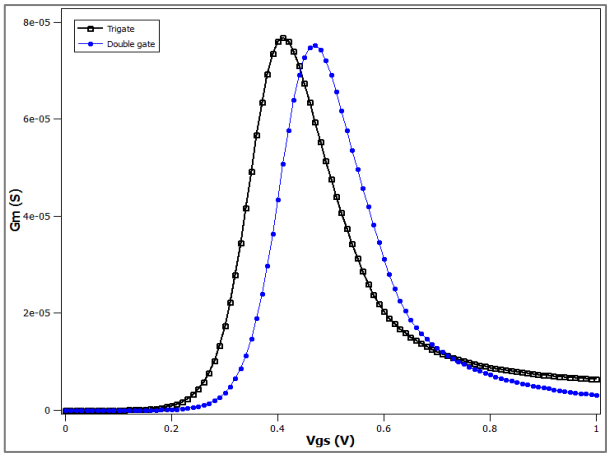

Figure 9: Transconductance vsVgs curve for n-type FETs

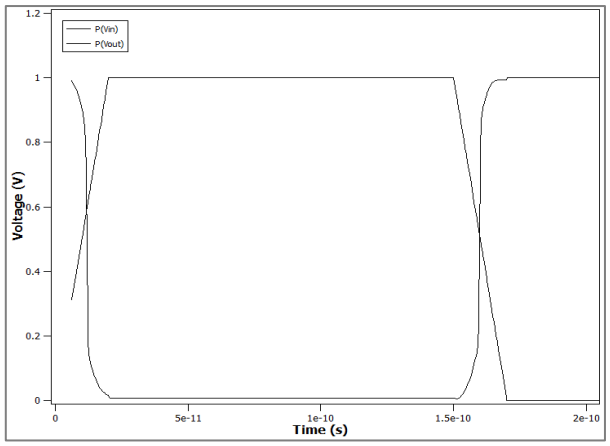

Figure 10: Simulated Waveform of DG FinFETs based Inverter

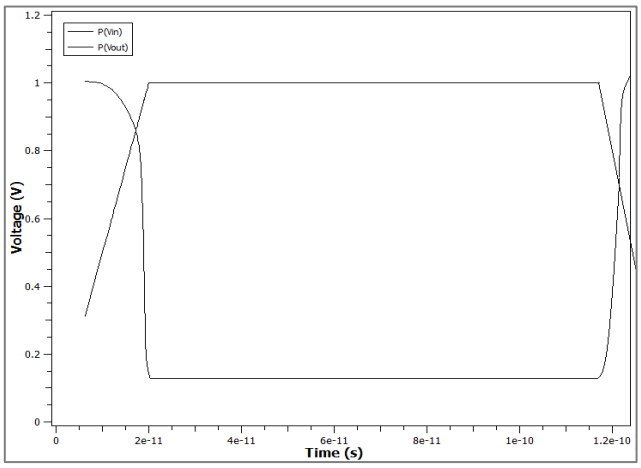

Figure 11: Simulated Waveform ofTrigateFinFETs based Inverter

TABLE 5: Inverter values

Parameters	**DG FinFETs based Inverter**	**TrigateFinFETs based Inverter**
Propagation delay	147ps	122ps
Noise Margin High	430mV	452mV
Noise Margin Low	474mV	489mV

CONCLUSION

Double gate, Trigate SOI FinFET devices and inverters based on these devices were successfully designed and simulated. Trigate structures shows more desirable performance in terms of I_{on} current, leakage current, switching speed(I_{on}/I_{off}ratio), minimum voltage required for conduction, DIBL, Transconductance and SSthan double gate FinFETs. Further inverter based on trigate devices demonstrates less delay and high noise margin which is essential for circuits.

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