A QUANTUM COST EFFICIENT REVERSIBLE 8 TO 1 MULTIPLEXER FOR LOW POWER APPLICATIONS

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ABSTRACT

Low power architectures are more pronounced for different applications that extend from Internet of Things to Quantum computing. Primitive combinational logic circuits induce from bit deletion due to information loss during the processing of input information which results in energy loss. The computations involving reversibility cancel the loss of information by sustaining the input bits from output. In the basic arithmetic and logic units, the combinational circuits play a significant role in determining the performance of the processor. The principals involved in the design of reversibility is an upcoming technology for ultra-low power applications. The reversible logic circuits furnish a thoroughly new way to progress in Quantum computing. In this article, we propose an energy tolerant low power reversible multiplexer with optimum energy loss. The proposed multiplexer also reduces the ancillae, garbage outputs and quantum cost considerably.

Keywords: Reversible logic gates, Mutliplexers, Computing,Power Consumption, Xilinx Software

I.INTRODUCTION

The rapid advancement of digital technology has escalated the demand for energy-efficient and high-performance computational systems. Traditional computing paradigms, primarily based on irreversible logic, are reaching their limits due to increased power consumption and heat dissipation. As a result, there is a growing interest in reversible logic, which offers a promising solution by minimizing energy loss through information preservation.Reversible logic is a computing paradigm where the input can be uniquely determined from the output, ensuring no loss of information. The development of a quantum cost-efficient reversible 8-to-1 multiplexer addresses these challenges, offering an innovative approach to designing low-power digital systems.This paper introduces a novel reversible 8-to-1 multiplexer designed for low-power applications, focusing on minimizing quantum cost while maintaining high efficiency. Our design leverages reversible logic gates to construct the multiplexer, ensuring minimal information loss and reduced energy dissipation. We conduct a comprehensive analysis of the quantum cost, delay, and garbage outputs of the proposed design, comparing it with traditional irreversible multiplexers and existing reversible designs.

Our work aims to contribute to the growing field of low-power digital design, demonstrating the feasibility and benefits of incorporating reversible logic into practical applications. By addressing the challenges of power consumption and efficiency, we hope to pave the way for more sustainable and advanced computing technologies.

II.LITERATURE SURVEY

The Proposed Multiplexer Architecture performs multiplexing operation. Multiplexers of various designs have already addressed and worked on by numerous authors in a literature of reversible designs with the aim of creating the large optimal and better performance circuits.

Performance evaluation of reversible logic gates" -- It has been realized that quantum computing is one of the latest technologies using reversible logic. It is observed that increasing growth of transistor density, power consumption will reach their limits in conventional technologies. In conventional Circuits during the logic operations bits of information is erased resulting dissipation of energy in significant amount. Thus, if Circuits are designed so that information bits can be preserved, the power use can be reduced. In case of reversible logic computation, the information bits are not lost. We can use reversible logic technology for minimizing the power consumption, heat dissipation, increasing speed etc. This paper describes various logic gates based on reversible logic like Toffoli, Peres, Fredkin, and Feynman etc. A

comparative between classical and quantum logic gates is also given on various parameters along with limitations of conventional computing.

III.PROPOSED DESIGN

For implementing an 8x1 Reversible Multiplexer, two 4x1 Reversible Multiplexer and one 2x1 Reversible Multiplexer are required which is as shown in below fig. This design quantum cost is twenty eight and produces 12 garbage outputs. The Reversible 8x1 Multiplexer is implemented based on the following equation.

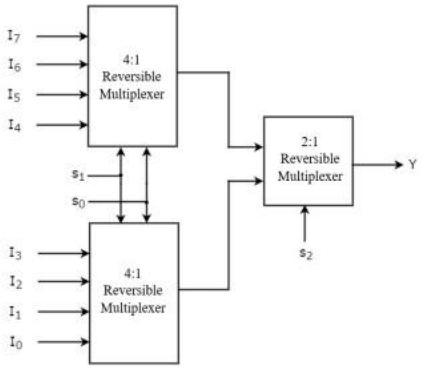
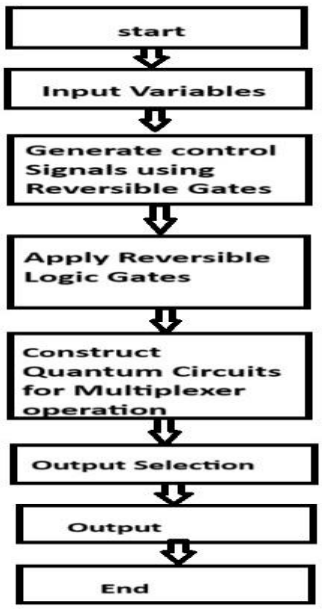


Fig: Proposed 8:1 Reversible multiplexer

Y=S2'S1'S0'I0+S2'S1'S0I1+S2'S1S0'I2+ S2'S1S0I3+S2S1'S0'I4+S2S1'S0I5+ S2S1S0'I6+ S2S1S0I7
Herewe are using S2 as most significant bit (MSB) among the three selection lines are used and S0 as least significant bit (LSB).

FLOWCHART



IV.RESULT AND SIMULATION

Truth Table For 8:1 Reversible Multiplexer

S0	S1	S2	Y
0	0	0	I4
0	0	1	I0
0	1	0	I5
0	1	1	I1
1	0	0	I6
1	0	1	I2
1	1	0	I7
1	1	1	I3

RTL SCHEMATIC OF 8:1 REVERSIBLE MULTIPLEXER:

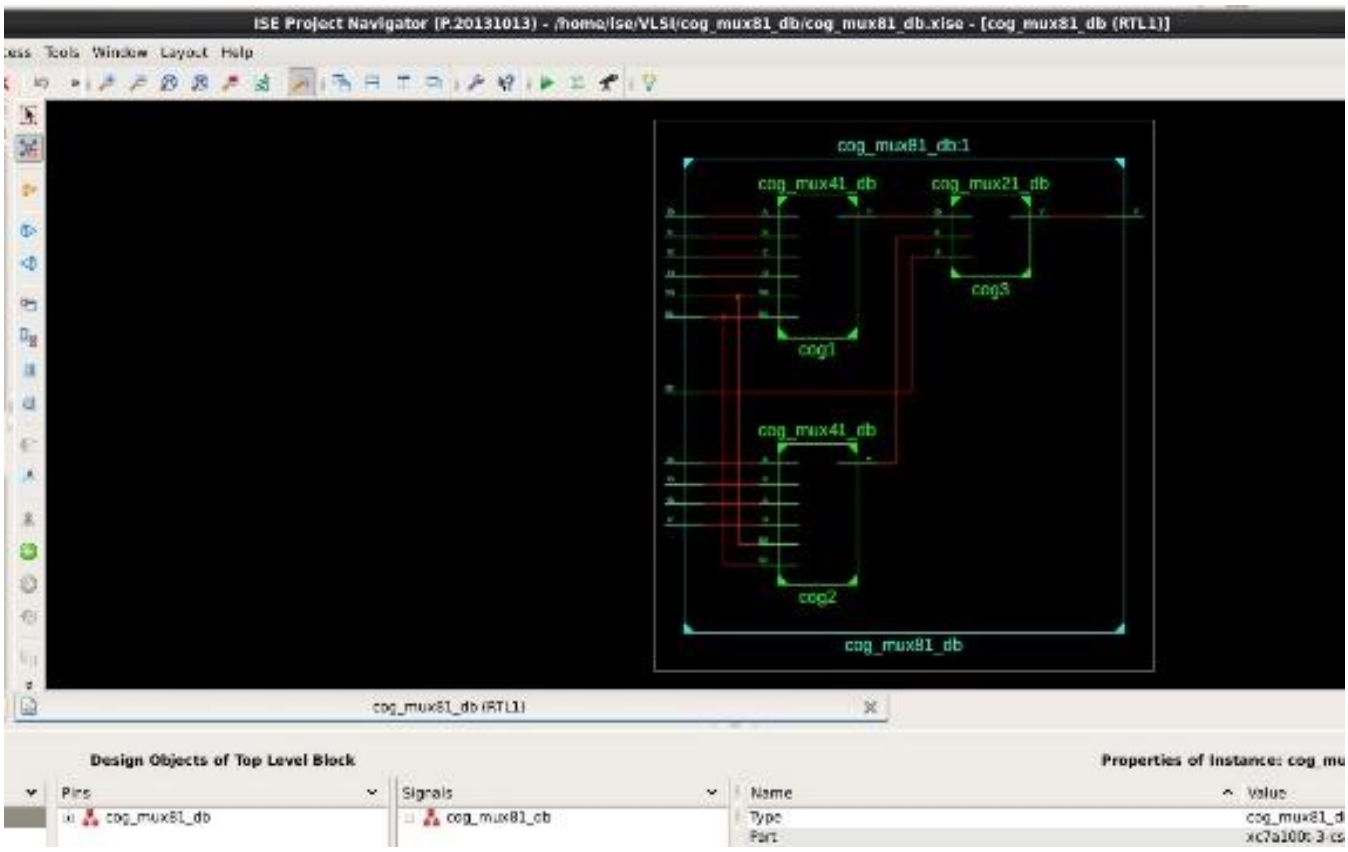


Figure.RTL Schematic Of Reversible 8:1Multiplexer

SIMULATION OF Reversible 8:1 Multiplexer:

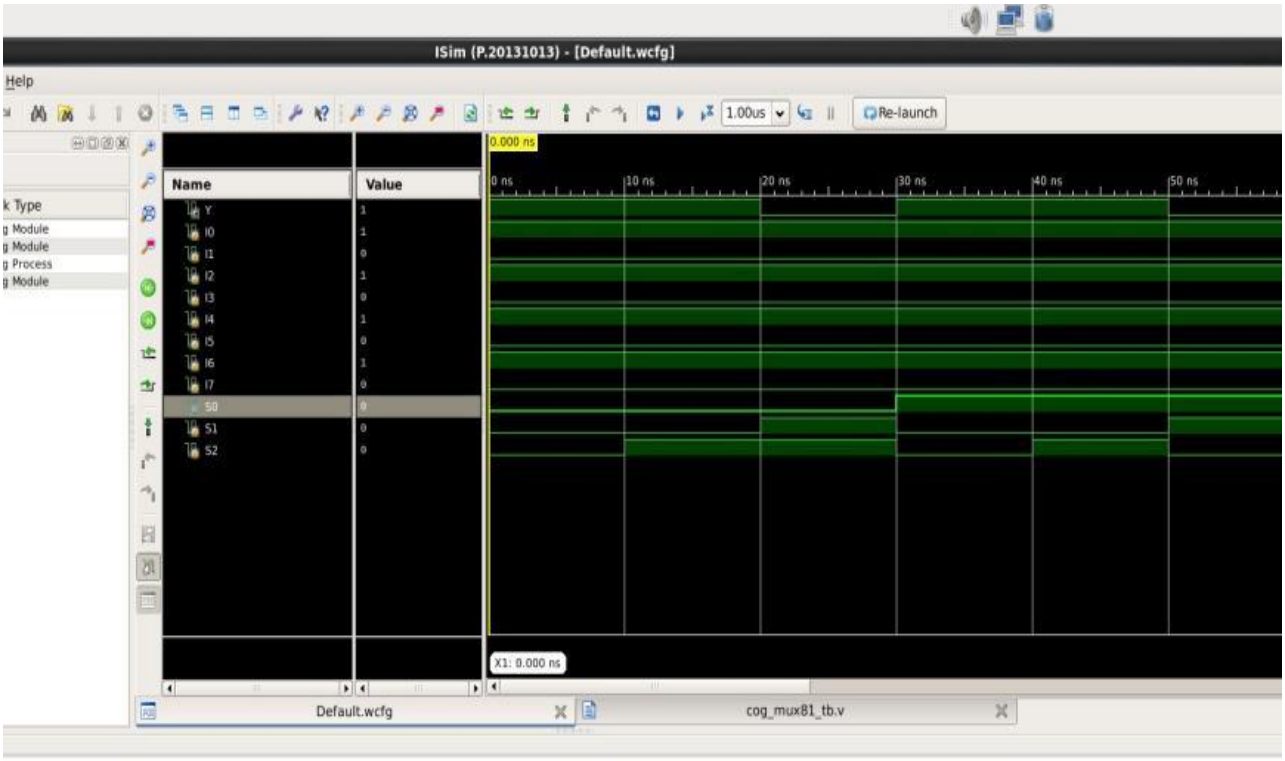


Fig.12. Simulation for Proposed Reversible 8:1 Multiplexer Design

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V TABLE

Table. Comparison of proposed design with existing Design

Parameters	**Existing Design**	**Proposed Design**
Flexibility	Low	High
Reversibility	No	Yes
Power Consumption	0.082 W	0.082 W
Time Delay	1.418 ns	1.354 ns

VI.CONCLUSION

The proposed design is a low garbage output design and it have a 12 garbage output values and 28 Quantum Cost.For computing system many conventional logic methods are available but, in reversible computing the input recreation is happened it is help to the applications of computing systems and the energy loss is avoided by the reversible logic gates.

VII.REFERENCES

When citing references for a research paper on a quantum cost-efficient reversible 8-to-1 multiplexer for low power applications, it is essential to include foundational works on reversible computing, quantum gates, and low-power circuit design. Here are some references that could be relevant:

1. Bennett, C. H. (1973). "Logical Reversibility of Computation."** IBM Journal of Research and Development, 17(6), 525-532. doi:10.1147/rd.176.0525.

- This foundational work discusses the principles of reversible computation.

2. Rai, R., Islam, S. M., & Hossain, M. A. (2013). "Efficient Design of Reversible Multiplexer and Demultiplexer Circuits."** International Journal of Computer Applications, 77(4), 13-17. doi:10.5120/13357-0931.

- This paper focuses on the design of efficient reversible multiplexers.

3.Thapliyal, H., & Ranganathan, N. (2010). "Design of Efficient Reversible Binary Subtractors Based on a New Reversible Gate."*IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 29(3), 395-398. doi:10.1109/TCAD.2009.2037505.

- This work discusses new reversible gates and their applications in efficient circuit design.

4.Singh, A. K., & Yadav, P. K. (2016). "Design and Analysis of Low Power Reversible Multiplexer Using Reversible Gates."** International Journal of Reconfigurable and Embedded Systems, 5(1), 39-46. doi:10.11591/ijres.v5.i1.pp39-46.

- This study explores the design of low power reversible multiplexers.