OPTIMIZED ARITHMETIC AND LOGICAL UNIT DESIGN USING REVERSIBLE LOGIC GATES

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ABSTRACT

In today's world, digital electronics are small and fast. However, the main problem with these systems is power consumption. There are different types of power supplies: static power supplies, dynamic power supplies, short-circuit blocking and power supplies. Power consumption plays an important role in VLSI circuit design. To reduce power consumption, various power consumption techniques are used, such as multiple Vth technology, clock gate, and inverse logic gate technology. The main advantages of using inverse logic devices for power generation are compatibility with the source and lack of heat generation by inverse logic devices. Arithmetic and logical units are the main components of a calculator. This article presents the design of an odd inverter arithmetic logic block, which consists of adder, subtractor and multiplier blocks. Design characteristics, waste, and quantum cost analysis. The design consists of 11 particles and 57 quantum values. The design was encoded in Verilog HDL and synthesized and simulated using Xilinx software.

Keywords: Reversible logic gates, Arithmetic Logical Unit Design(ALU), Computing,Power Consumption, Xilinx Software

I.INTRODUCTION

Irreversible gates are used as design units in the conventional techniques for creating a digital circuit. Due to bit loss in each operation, these gates cause information loss. The major source of heat produced by digital systems is the bit loss phenomenon in digital circuits.

Although it is true that computers consume a maximum energy, the question is why computers consume the maximum level energy? In 1961[1], Mr. Rolf Landauer developed a novel solution from thermodynamics for this problem that he named the Landauer principle. The principle demonstrates that irreversible information loss of every bit will result in the generation of the ln2kT Joules of heat energy, where ln is a logarithm of 2, T is a temperature, and k is the Boltzmann constant. In 1973, Bennett[2] demonstrated that using reversible computing as opposed to irreversible calculation prevents the expenditure of ln2kT Joules of energy.

[3] In typical computers, the calculation is irreversible, meaning that once the output is produced, the input data may be lost and cannot be recovered, resulting in increased power usage. Reversible logic circuits, however, are an exception to this rule since they allow for the generation of input from output. There will be a distinct input combination for each output logic. Because they are all multiple level input, single input to output logic gates, gates like AND, OR, and XOR cannot be reversed.

If the vectors of the input bits and output bits are equal and the inputs and outputs are assigned to each individual input in a one-to-one relationship, then a logic gate is said to be reversible. Information cannot be deleted using reversible logical processes, and no heat is produced. [5] In order to reproduce the inputs from the outputs, the reversible circuit works backward, which results in zero power usage. Reversible logic gates are used to create reversible circuits, which carry out difficult logical and arithmetic operations. From the help of Reversible Logic gates (toffoli, peres gate [6]) the Arithmetic and Logical unit is proposed. This ALU design is Consists a Peres gate based Reversible adder, DKG gate based subtractor and Reversible 2x2 multiplier. Also, the proposed ALU design is combined with a decoder, Multiplexer and 1 bit memory unit.

II. LITERATURE SURVEY

The Proposed ALU Architecture performs the addition, Subtraction and multiplication operations and additionally decoder and multiplexer is combined. Adder, Subtractor and multiplier of various designs have already addressed and worked on by numerous authors in a literature of reversible designs with the aim of creating the large optimal and better performance circuits [7-10]. In the year 2011[7], S. Sultana optimised this 8-bit Adder/Subtractor architecture. They used twenty-five reversible logic gates, seventeen trash outputs, and seventy three quantum rate while designing this circuit. An improved 4-bit Adder/Subtractor [8] circuit was put out in the 2013 publication by, Shefali Mamataj. 8 reversible gates with a mix of

Feynman and DKG gates were used in that design. 11 trash output signals were produced by this design. In 2015, Harpreet Singh [9] suggested a novel reversible logic gate under the moniker WG gate. This paper presents the construction of a comprehensive Adder/Subtractor circuit utilising with a one gate and two trash outputs and a quantum rate of seven. In [10] the adder/subtractor design is proposed using reversible gates .

In 2018 [11], the HNG gate based 8 bit and 4 bit array multiplier is proposed. The author proposed the multiplier design using HNG gate based Ripple Carry Adder and the multiplier design have a 28 gates, 5249 nW power, 231 µm2 area.

In 2017 [12], the sixteen bit reversible arithmetical and logical unit is design by the author Swaminathan. The ALU design contains adder and subtractor and the multiplexer is used as a
control unit.

In 2021[13], the novel ALU design is provided by the author BehrouzSafaiezadeh using quantum dot cellular automata. The proposed design performs 6 Arithmetic operations and 10 logical operations. The design is reduced the area 0.92 µm2 to 0.62 µm2 and Quantum rate 21 to 16 compared to other existing designs and Vedic multiplier design[14] is designed using Quantum Dot cellular automata.

In 2011 [15], the author approach the two different ALU designs and comparison of the ALU parameters also provided. The Quantum rate is reduced compared to the other existing designs.

In 2020 [16], author Ravi Ranjan provide the 8 bit reversible ALU Architecture on programmable gate. In this design the adder/subtractor performance is increased.

In [17] the reversible gates and combinational circuits are reviewed and the author gave the difference of the combinational circuits design using multiple reversible logic gates. Above literature survey shows that, the researchers have done particular work in area of reversible logic based circuits and ALU designs. This paper presents a low garbage output reversible Arithmetic and logical unit architecture.

III. PROPOSED DESIGN

The Reversible arithmetic and logical unit architecture is proposed. Generally, the arithmetic system performs the addition, subtraction and multiplication operations. The proposed combined architecture contains the adder, subtractor, multiplier, 1 bit memory store element edge triggered flipflop[18], encoder, multiplexer and logical unit. For the adder design Peres gates are used. In full adder design sum and carry generation is not possible without copying one of the inputs. In reversible logic overlap of the input information help to generate the carry and sum in garbage bits. Different reversible adders are used in the ripple structure [19]. e.g. reversible binary coded decimal adder. For single bit adder design 2 gates are used. For 4 bit, 8 gates are used. For n bit, 2xn-bit size gates are used. For Subtractor 4x4 DKG gate is used. Multiplication is a another important operation for computing system. To perform the multiplication operation in reversible, save both multiplicand and multiplier while still producing the product .

For storing the bit, 1-bit memory store element edge triggered flip flop is proposed and shown in figure . In this proposed design, decoder and multiplexer combined with ALU architecture

For storing the bit, 1bit memory element reversible edge triggered flip flop [20] is used. The combined method of ALU is approached from the implementation of De interleaver. It performs the addition, subtraction and multiplication operations in single cycle and simulation of the operations and RTL view of the design shown below .

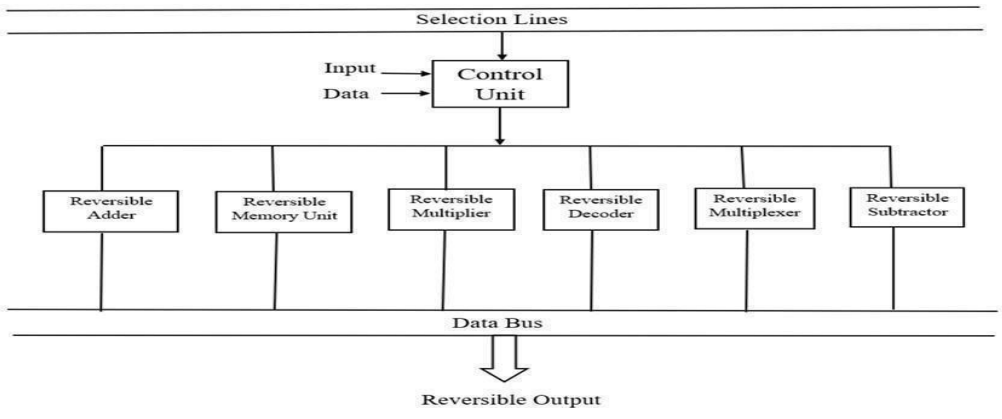
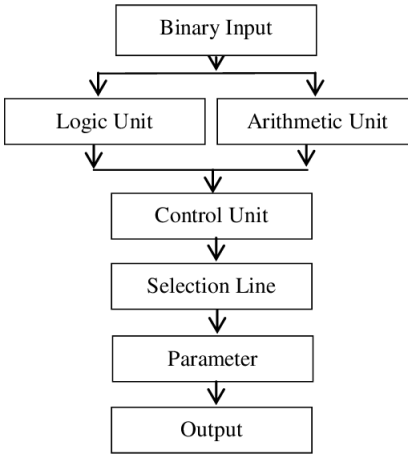


Fig.1. Proposed Combined ALU Architecture

IV. FLOW CHART



V. SIMULATION AND RESULTS

Second and third output of the 1st Gate is connected with a 2nd Peres gate input pin 1 and 3. Pin 2 is connected with input Carry. The output of the adder Sum and carry out is produced in 2nd Peres gate pin 2 and 3. In simulation, the adder input pins a is set as 1, b set as 0 and Cin set as a 1. The output of the adder sum and Carry out is generated in the pin sum and Cout as 0 and 1. The full adder have a 1 trash output, 8 quantum rate and 6 number of gates. The synthesized design and simulation is shown in figure. The full subtractor circuit is design is constrcted using DKG reversible gate. For performing full subtraction operation in DKG gate, input pin 1 is declared as 1, pin 2&3 connected with a subtractor input a and b, borrow input is connected with pin 4. The output Borrow out and difference is produced at the DKG gate 3&4. In simulation figure.16, the input pins of the gate, a is set as 0, b is set as 1 and Bin set.

1st gate is produced the output P0 at pin3. Output of the 2nd and 3rd Toffoli gate is connected with a half adder design1 and half adder design1 output at pin 2 and 4th gate output is connected with a half adder design2. Half adder design1 and design2 is produced the output of the multiplier P1, P2 and P3.

RTL SCHEMATIC OF ALU:

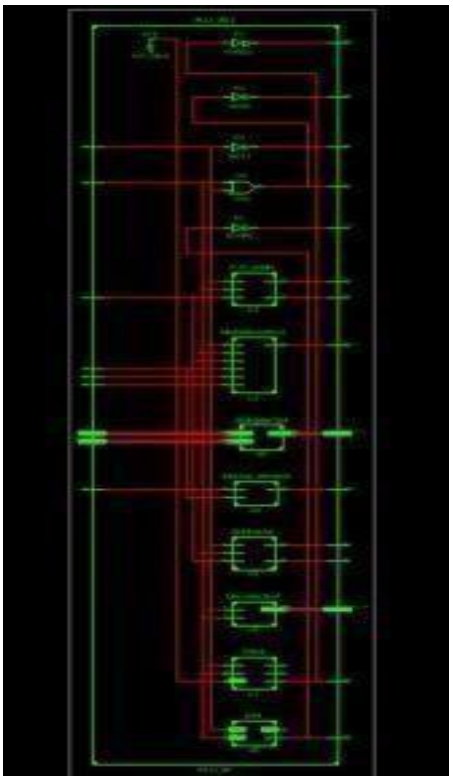


Fig.2. Synthesize Circuit Proposed ALU Design

SIMULATION OF ALU:

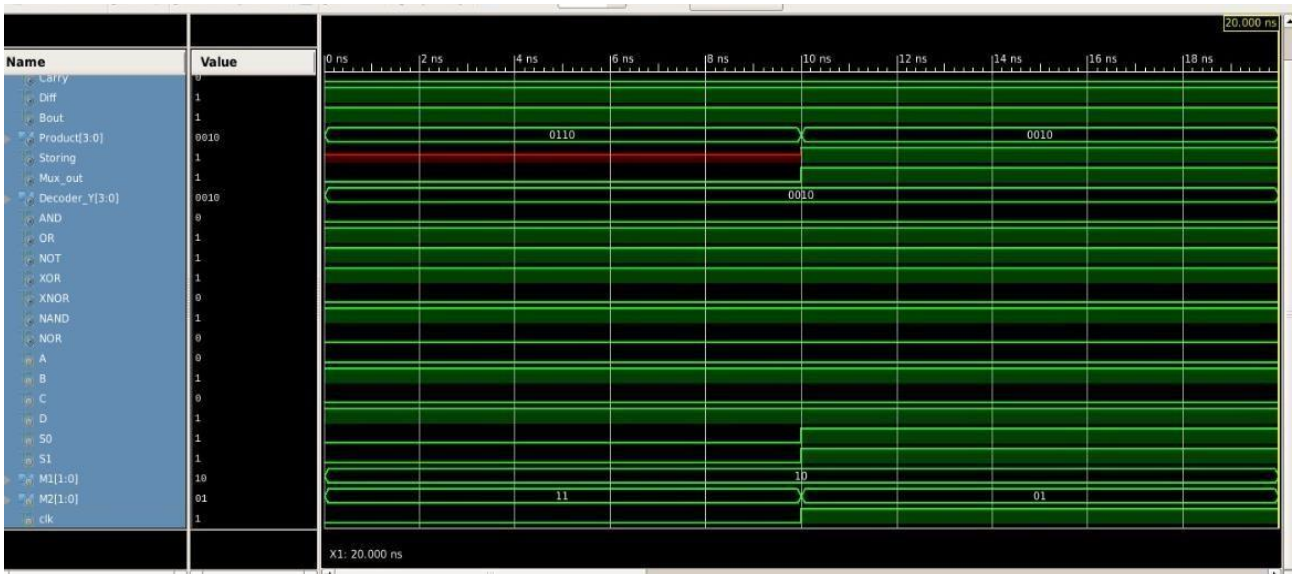


Fig.3. Simulation for Proposed ALU Design

The subtractor have a 2 trash outputs and 17 quantum rate, the multiplier has a 8 trash output values and 32 quantum rate. Totally the proposed design contains the 11 trash outputs and 57 quantum cost.

VI TABLE

Table. Comparison of proposed design with existing Design

Parameters	**Existing ALU Design**	**Proposed ALU Design**
Quantum Cost	28	57
Garbage Output	18	11
Power Consumption	0.140 W	0.082 W
Time Delay	2.041 ns	1.071 ns

VII. CONCLUSION

The proposed design is a low garbage output ALU design and it have a 11 garbage output values and 57 Quantum Cost. This design is dedicated to the computer arithmetics. For computing system many conventional logic methods are available but, in reversible computing the input recreation is happened it is help to the applications of computing systems and the energy loss is avoided by the reversible logic gates.

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