DESIGN AND IMPLEMENTATION OF LOW QUANTUM COST REVERSIBLE UNIVERSAL SHIFT REGISTER

*[1]Dr.K.H.Shakthi Murugan, Associate Professor , [2]Pygala Sravya Sri, [3]Raavi Sravani,
[4]Durbhakula Nithya Sri, [5]Pamujula Sucharitha
Department of ECE Narayana Engineering College,Gudur

ABSTRACT

The project proposes an efficient design of a 4-bit Reversible Universal Shift Register (RUSR) using Reversible Logic Gates. RUSR performs shifting operations the same as CMOS-designed universal shift registers, such as left shift, right shift and parallel load, respectively. In this project, we are designing a 4-Bit RUSR using a Reversible MasterSlave D-Flipflop (RMSDFF) and Reversible 4X1 Multiplexer (RMUX41). The proposed RMSDFF and RMUX41 are designed using Feynman (FG), Fredkin (F) and Modified Fredkin (MF) gates. Modified Fredkin gate plays a remarkable role in the implementation of the proposed optimized architecture. The efficiency of the proposed architecture is demonstrated in terms of Garbage Outputs (GO) and Quantum Cost (QC). The proposed architecture reduces the power consumption with a low quantum cost, a minimum number of reversible logic gates and garbage outputs. Due to this, the proposed design is particularly beneficial in Quantum Computing, Low-power CMOS design, and other applications. In this project, the RUSR is designed by the proposed RMUX41 and RMSDFF, which are designed with the reversible logic gates using VHDL and verified with the simulated results using the Xilinx 14.7 ISE tool.

Key words-Quantum Computing,Quantum Cost,Low power CMOS,Universal Shift Register, Reversible logic gates,Garbage Outputs.

I. INTRODUCTION

Reversible Computing is a model of computing where the computational process to some extent is reversible, *i.e.*, time-invertible. In a model of computation that uses deterministic transitions from one state of the abstract machine to another, a necessary condition for reversibility is that the relation of the mapping from (nonzero-probability) states to their successors must be one-to-one. Reversible computing is a form of unconventional computing. Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R. Landauer in the year 1960. According to Landauer's principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann's constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin[1]. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennett, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2].

According to Moore's law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information.The most prominent application of reversible logic lies in quantum computers . A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing .

Quantum networks composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence

quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).

Thus, quantum arithmetic must be built from reversible logical components [3]. Reversible computation in a system can be performed only when the system comprises of reversible gates. A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments [4-6]. An N*N reversible gate can be represented as
Iv=(I1,I2,I3,I4,.....IN)
Ov=(O1,O2,O3,.....ON)
There are many number of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter.

Irreversible gates are used as design units in the conventional techniques for creating a digital circuit. Due to bit loss in each operation, these gates cause information loss. The major source of heat produced by digital systems is the bit loss phenomenon in digital circuits.Although it is true that computers consume a maximum energy, the question is why computers consume the maximum level energy? In 1961[1], Mr. Rolf Landauer developed a novel solution from thermodynamics for this problem that he named the Landauer principle. The principle demonstrates that irreversible information loss of every bit will result in the generation of the ln2kT Joules of heat energy, where ln is a logarithm of 2, T is a temperature, and k is the Boltzmann constant. In 1973, Bennett demonstrated that using reversible computing as opposed to irreversible calculation prevents the expenditure of ln2kT Joules of energy.

II. LITERATURE SURVEY

Rajeshwari, M., Rohini S. Hongal, and Rajashekar B. Shettar. ”Design and Implementation of 8 Bit Shift Register using Reversible Logic.” 2018 International Conference on Current Trends towards Converging Technologies (ICCTCT). IEEE, 2018. Power dissipation is becoming major problem as device size is shrinking. Conventional circuits are irreversible in nature and dissipates power for every bit loss in circuit. Instead if we use reversible logic power dissipation can be reduced. The paper is intended to design and implementation of 8-bit shift register using reversible logic gates on FPGA board using chipscope. The proposed 8-bit shift register using reversible logic is optimized in terms of quantum cost, delay, number of logic gates used. Quantum cost of the proposed design shows up to 8% improvement and in comparison with existing work in survey. The coding is done using verilog module then simulated using Xilinx Modelsim and prototyped in Spartan6 board using real time tool chipscope for verification of result.

III. METHODOLOGY

A.PRINCIPLES OF REVERSIBLE COMPUTATION

Reversible Gate: A logical gate is referred to as reversible if it contains an equal number of inputs and outputs. A reversible gate is also known as a reversible circuit with n inputs and n outputs.

Quantum Cost (QC): Quantum cost is used to represent the cost of a reversible circuit. Cost is calculated based on the number of quantum gates used to develop a quantum circuit. A reversible gate has its own quantum cost which is determined by the no. of basic reversible logic gates (1x1 or 2x2) needed to implement the circuit.

Garbage Outputs (GO): Garbage output can occur in reversible computing when there are unused or unneeded bits or signals that are produced as part of the computation.

B.SOME BASIC REVERSIBLE LOGIC GATES AND THEIR QUANTUM IMPLEMENTATION

Reversible Gate: A logical gate is referred to as reversible if it contains an equal number of inputs and outputs. reversible gate is also known as a reversible circuit with n inputs and n outputs.

Quantum Cost (QC): Quantum cost is used to represent the cost of a reversible circuit. Cost is calculated based on the number of quantum gates used to develop a quantum circuit. A reversible gate has its own quantum cost which is determined by the no. of basic reversible logic gates (1x1 or 2x2) needed to implement the circuit

Garbage Outputs (GO): Garbage output can occur in reversible computing when there are unused or unneeded bits or signals that are produced as part of the computation. These can include temporary variables, intermediate results, and other data that is not needed for the final output of the computation.

Fredkin Gate (FG) :It is also known as the Controlled- Swap gate. It is a threequbit gate that swaps the 2nd and 3rd qubits if the 1st qubit is in $|1\rangle$ state as shown in figure 1. The state will be unchanged if the 1st qubit is in $|0\rangle$ state. Quantum Implementation of FG is as follows.

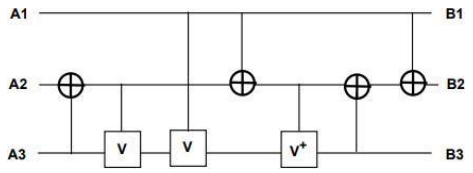


Fig. 1. Quantum Implementation of Fredkin gate

Modified Fredkin Gate (MF): It is also known as the Controlled-Swap gate with Ancilla (CSWAP-A) or Toffoli-Fredkin gate. As shown in figure 2, It performs a controlled swap operation between the 2nd and 3rd qubits, controlled by the 1st qubit state by leaving the 4th qubit unchanged. Quantum Implementation of MF Gate is as follows.

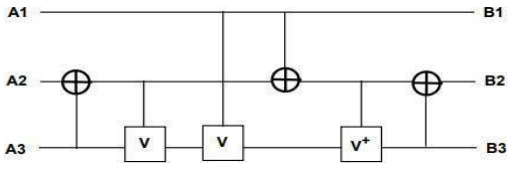


Fig.2:Quantum Implementation of Modified Fredkin Gate

In quantum computing, these gates can be implemented using various physical systems, such as trapped ions, superconducting qubits, or photonics. The exact implementation of these gates can vary depending on the specific physical system being used, but the underlying mathematical principles are the same.

IV. PROPOSED WORK

The working of a Universal Shift Register has been demonstrated in many existing designs. In these designs, various reversible gates are used to implement various components. The proposed 4-bit RUSR is designed using the proposed Reversible 4x1 Multiplexer (RMUX41) and Reversible Master-Slave D-Flipflop (RMSDFF). To design RMUX41, the MF gate (MF) is used and to design the RMSDFF, MF gate and F gate are used.

a. **Reversible 4-Bit Universal Shift Register (RUSR) :**The proposed Reversible 4-Bit RUSR has both left and right shifts and parallel load capabilities. The mode of operation of the register depends on the selection inputs S0 and S1, as shown in Table I.

TABLE I
FUNCTION TABLE FOR 4-BIT RUSR

S1	S0	(Operation) Final Output
1	1	(Parallel Load) In[i]
1	0	(Left Shift) Q[i+1]
0	1	(Right Shift) Q[i-1]
0	0	(No Change) Q[i]

As shown in Table I, When the inputs S1 and S0 are low, D inputs of the RMSDFFs are fed with the current value of the register. The above condition creates a path from each RMSDFF output into the same RMSDFF input. The next clock pulse is given with the previous value to each RMSDFF.

The proposed 4-Bit RUSR is illustrated in Figure 3. As shown in Figure 3, the serial input for the left shift for the first stage is SINL and the serial input for the right shift for the last stage is SINR. The proposed 4-bit RUSR is designed using four RMSDFF and four RMUX41, respectively with the cost of the quantum gates (QC) of 98 and 20 GOs.

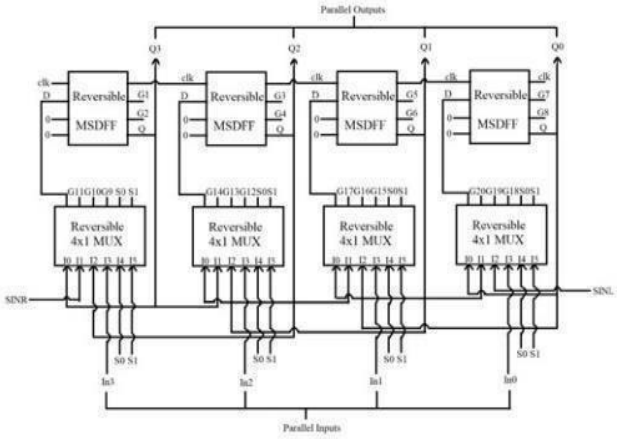
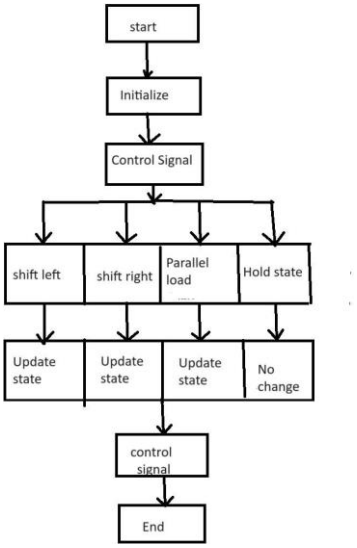


Fig.3:Block Diagram of 4-bit RUSR with Reversible Logic

b. Flow Chart of the Proposed System:

A flowchart for a reversible universal shift register outlines the step-by-step process and logic flow for shifting data in different directions and modes.



V. RESULT ANALYSIS

The proposed design RUSR consists of components such as sequential unit such as RMSDFF which is used as memory, shift register and shift unit such as RMUX41 to work for shift operations according to the select lines. The top-level entity of design consists of one 4-Bit input which is parallel inputs In, one 2-Bit input which are selection inputs S, two inputs such as SINL, SINR for inputs of serial left shift and right shift respectively, one clock input and, some constant 1'b0 inputs. VHDL code for all modules are written and the final outputs for every negative edge of clock pulse are simulated using XILINX Tool. Simulation result of the Final proposed top module, which is 4-Bit RUSR is shown in Figure 5.

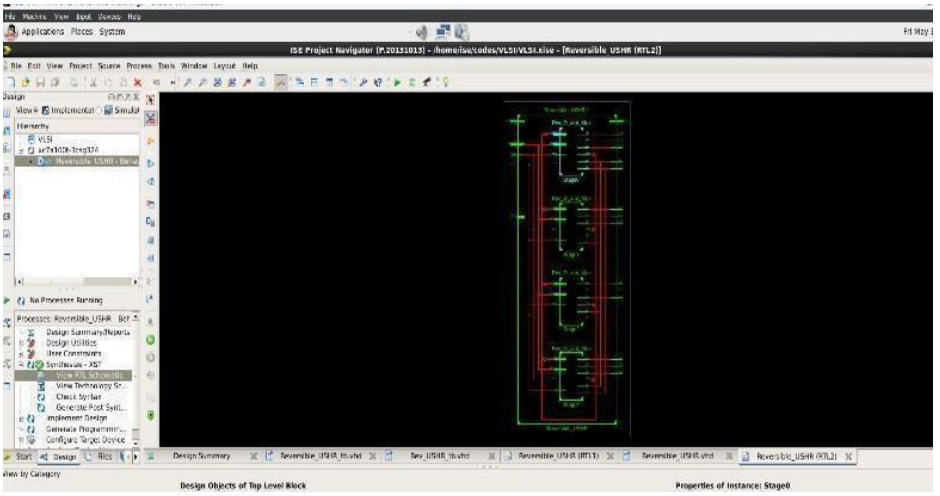


Fig.4:RTL Schematic of Reversible Universal Shift Register

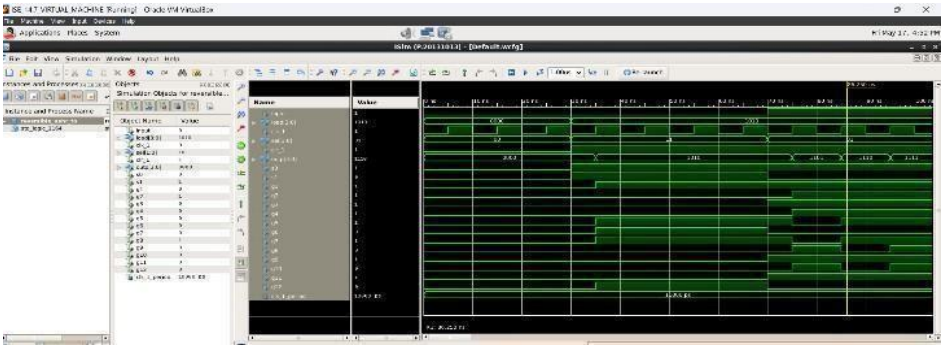


Fig.5:Simulation of 4 bit Reversible USR

Table 2

Difference Between Proposed system and Existing System

Parameters Flexibility Low High	Existing System	Proposed System
Power Dissipation	0.14W	0.082W
Time Delay	2.987ns	1.005ns
Reversibility	No	Yes
Flexibility	Low	High

VI. CONCLUSION

The Universal Shift Register is an important sequential memory element. In this project, we proposed a novel approach of designing an Optimized Reversible Universal Shift Register with the help of proposed Reversible Master- Slave D-Flipflop (RMSDFF) and Reversible 4X1 Multiplexer (RMUX41). The proposed RMSDFF and RMUX41 are designed using Feynman (FG), and Modified Fredkin (MF) gates. Our proposed design is better than the existing ones in literature in the factors such as QC, No.of gates, GOs. This optimization necessarily adds an advantage to the reversible logic community.

REFERENCES

[1] R. Keyes and R. Landauer, "Minimal energy dissipation in logic," IBM Journal of Research and Development, vol. 14, pp. 152-157, 1970.

[2] R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, pp. 183- 191, 1961.

[3] G. E. Moore, "Cramming more components onto integrated circuits," Journal of Electronics, vol. 38, no. 8, pp. 114-117, April 1965.

[4] C. H. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, vol. 17, no. 6, pp. 525-532, 1973.

[5] C. H. Bennett, "Notes on the history of reversible computation," in IBM Journal of Research and Development, vol. 32, no. 1, pp. 16-23, Jan. 1988, doi: 10.1147/rd.321.0016.

[6] N. Srinivasa Rao, P. Satyanarayana (2017). Design and Synthesis of Multiplexer based Universal Shift Register using Reversible Logic. IOSR Journal of VLSI and Signal Processing. 07. 08-13. 10.9790/4200- 0703010813.