A LOW-POWER AND RECONFIGURABLE 16-BIT ADDER USING REVERSIBLE GATES

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ABSTRACT

One of the most well-known technologies that is making a bigger contribution to current technological environment is DSP systems. With multiple applications, such as readily transportable electronic gadgets, the system that accepts films and audio as input, etc., embedded systems have gained popularity all over the world. The project is mainly focused on low-power, efficient, and programmable adders. Reversible logic gates, which are mostly employed for designing, provide the basis of this adder. The adders are developed and implemented using the Xilinx tool. These adders can be used in aerospace applications. There was a comparison made between the current and proposed methods in that the proposed way resulted in a reduction of 2005.34 nanowatts compared to the existing method.

Key Words: Field Programmable Gate Array (FPGA), Error Tolerant Adder (ETA), Toffoli gate, Reversible gates,Power Optimization, Reconfigurable , Low Power Adder(LPA).

I. INTRODUCTION

In recent years the computing resources like FPGA, CPU deploys various kind of operations. So, there is a need for designing Reconfigurable adders which is used in image processing and error tolerant applications. In digital design energy loss is considered as important factor. The logic circuits which are traditionally designed uses irreversible logic gates and they also dissipate heat energy. The reduction of area, power and latency is done using various techniques. Reversible logic is one such technique which is used to design combinational and sequential circuit. Reversible gates are considered as the building block of any reversible circuit. The characteristics of reversible gates are given as follows. It has same number of input and output so that it can have one-to-one mapping [5]. The reversible gates have a uniquely identified input as well as output. Reversible gates such as BJN and Toffoli are proven to reduce the power dissipation. BJN and Toffoli gates are used instead of Conventional logic gates. Traditional logic synthesis methods cannot be directly used for construction of reversible gates. Reversible gate has an important characteristic that is garbage output. The initial output or any gate is usually provided with an input that is taken from garbage output In reversible logic the one-to-one mapping can be accomplished by having gate output which is like that of inputs. For set of input vectors, this produces a unique set of output vectors. This prevents information loss, which results in power loss.

II. LITERATURE SURVEY

Many different adders were used previously to achieve an increase in efficiency of area, power, and speed.Conventional logic gates have many inputs and only one output. Reversible gates are gates having the same number of inputs and outputs[5]. This property of the same number of input and output results in less power dissipation[7]. There are many different types of reversible gates[1]. Some of them are BJN, Toffoli, Feyman, Peres gate, etc.Error Tolerant Adder has been used to increase the efficiency of area, power, and speed.Variable Accuracy Reconfigurable Adder (VARA) was used to consume less power than the traditional CSLA(Carry Select Adder). The HPVARA architecture, alternatively, is proposed for hybrid packages that may take delivery of correct and faulty representations to attain super pace, vicinity, and power[3]. All the above-discussed adders are designed using logic gates. The proposed Reconfigurable Reversible Low Power Adder is designed using reversible logic gates for better efficiency.

III. METHODOLOGY

1.BJN

BJN is employed as an all-purpose gate. Additionally, known as Modified Toffoli Gate, BJN. A 3x3 reversible gate is shown in the figure.

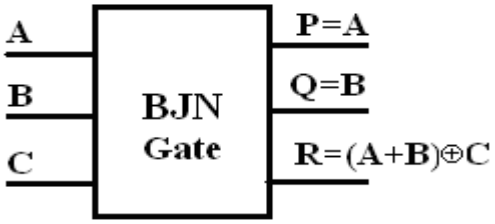


Fig. 1 BJN Gate

2.Toffoli

The reversible gate family includes the toffoli gate which is depicted in the figure. The "controlled-controlled-not" (CCNOT) gate is another title for it. Reversible gates are frequently utilized since there is absolutely no danger of data loss and heat dispersion is noticeably extremely low. Information is not lost by the gate while calculation is taking place. It operates on three qubits. One control and two targets make up the gate. The cost of the Toffoli gate quantum is 5. The gate may be used to build any reversible gates. The first bits are set to 1 and the third bit is inverted since all the bits remain unchanged.

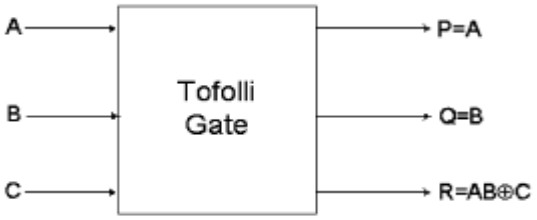


Fig. 2 Toffoli Gate

IV. PROPOSED DESIGN

The proposed Reconfigurable Reversible Low Power Adder is depicted in figure 1, it can be used to reduce the power consumption.The 16-bit low power adder consist of 4 RCFA_RCHA modules and 3 ARCFA modules and 3 CE modules.Reversible logic gates are used instead of traditional logic gates in-order to achieve low power consumption. Three RCFA modules and one RCHA module make up the RCFA-RCHA module. RCFA resembles a full adder in most ways. The only difference between it and a full adder is that it makes errors in the carry and sum output on each of the eight occasions that it occurs.When compared to traditional CFA, the RCFA keeps two gates and two delayed gates.

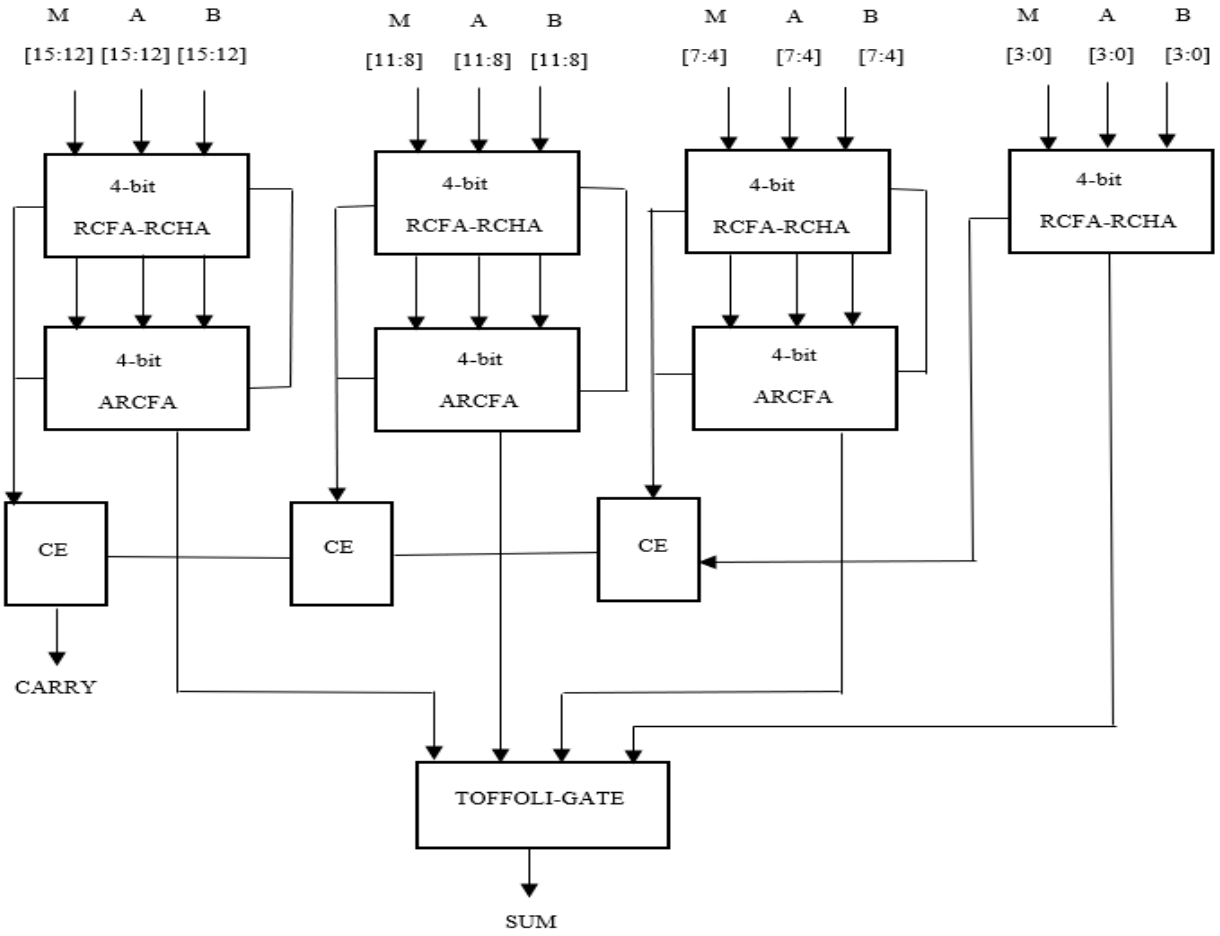


Fig. 3 Schematic diagram of Proposed Reconfigurable LPA using reversible gates

Xilinx software: Software from Xilinx is used to design and simulate embedded applications. It is often a tool for HDL generation and analysis.

V. SIMULATION RESULTS

The results of the reversible gate with low power have been reviewed and explained. The proposed reversible reconfigurable adder is synthesized with xilinx compiler . The modules in the proposed are programmed using VHDL in Xillinx ISE.

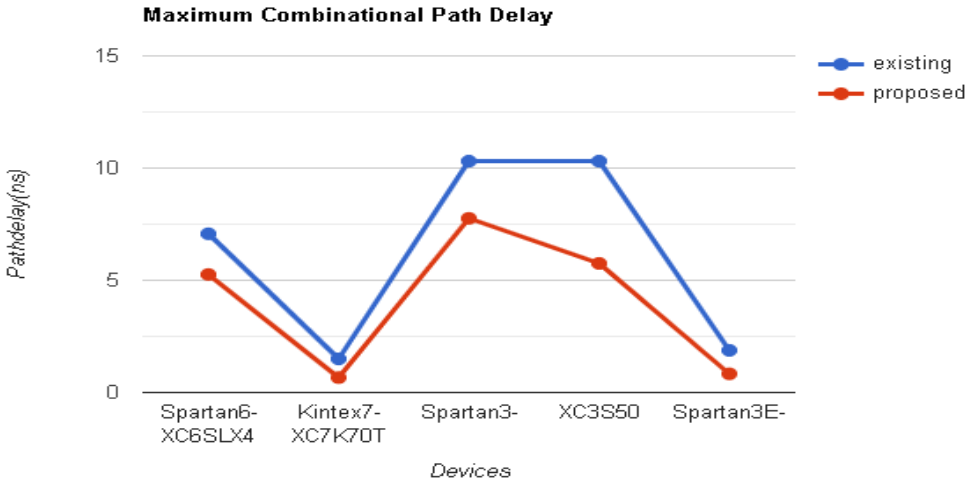


Fig. 2 Max. Combinational Path delay

The above graph depicts the maximum combinational path delay in nanoseconds by the existing HPVARA and proposed RRLPA which shows that the maximum combinational path delay in RRLPA is lower than that of HPVARA.

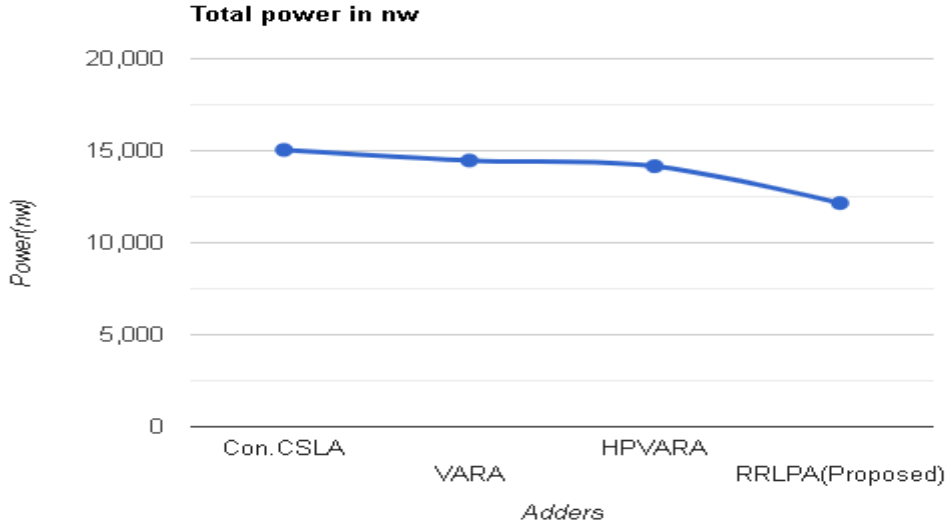


Fig. 3 Total power

The above graph depicts the total power in nanowatts used by different adders such as conventional CSLA, VARA, HPVARA and proposed RRLPA which shows that the total power used is reduced in proposed RRLPA. This

graph is obtained by calculating the total power (nanowatts) in each of the different adders using Xilinx tool. Figure 3 depicts the graphical comparison of total power in nanowatts.

Proposed RTL Schematic Diagram

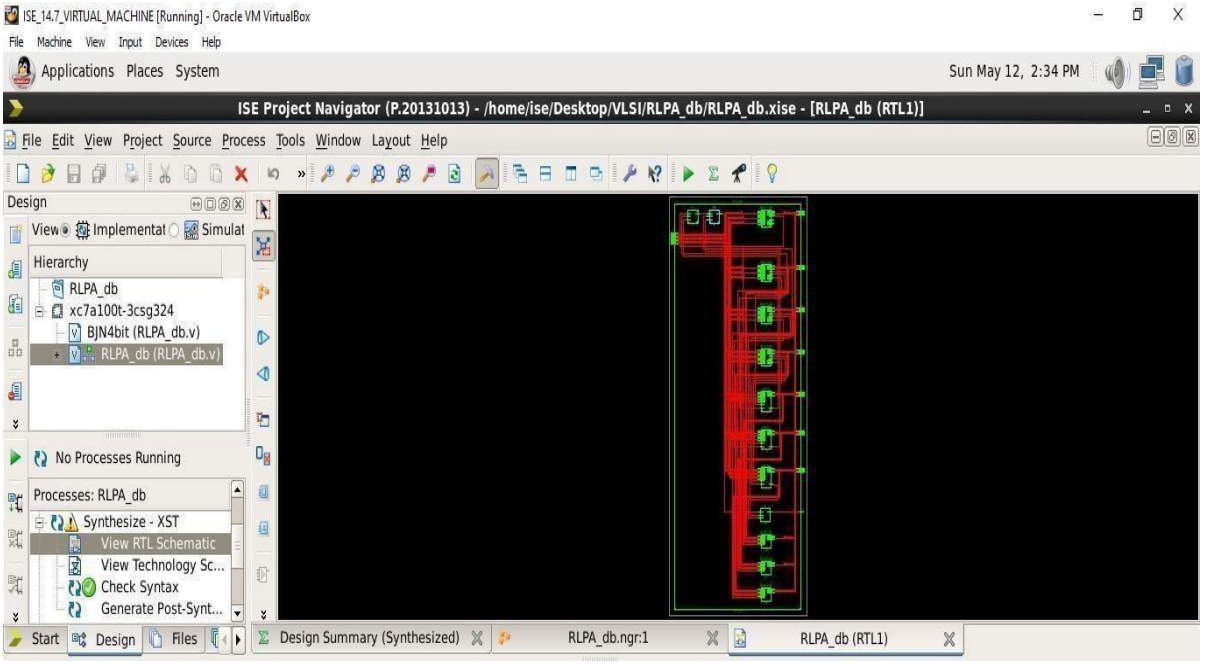


Fig. 4 RTL Schematic Diagram

Proposed Timing diagram

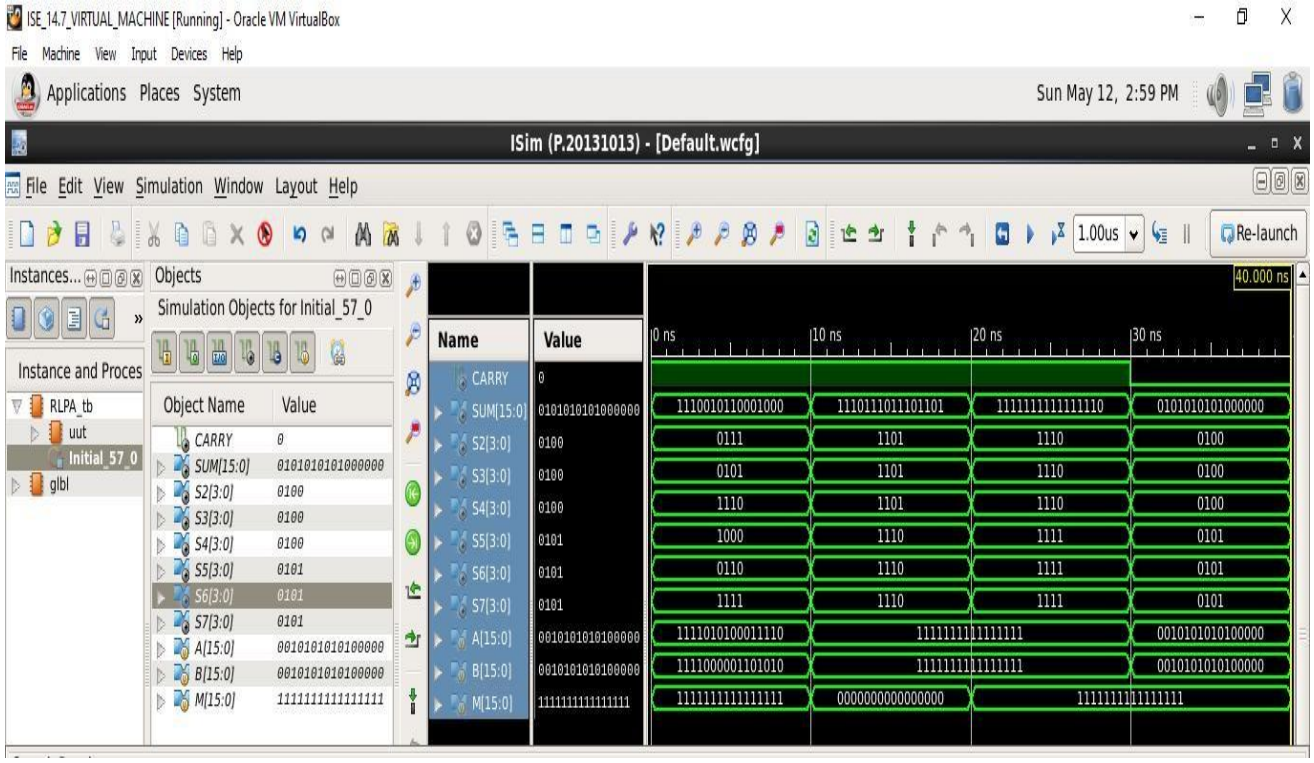
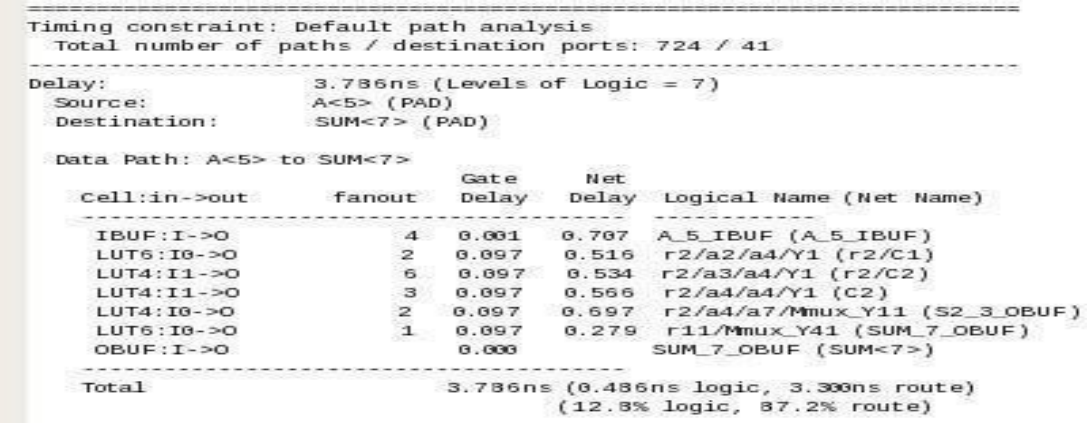


Fig. 5 Simulation Timing Diagram



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Timing constraint: Default path analysis
  Total number of paths / destination ports: 724 / 41
--------------------------------------------------------------------------------
Delay:               3.786ns (Levels of Logic = 7)
  Source:            A<5> (PAD)
  Destination:       SUM<7> (PAD)

  Data Path: A<5> to SUM<7>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             4   0.001   0.707  A_5_IBUF (A_5_IBUF)
     LUT6:I0->O            2   0.097   0.516  r2/a2/a4/Y1 (r2/C1)
     LUT4:I1->O            6   0.097   0.534  r2/a3/a4/Y1 (r2/C2)
     LUT4:I1->O            3   0.097   0.566  r2/a4/a4/Y1 (C2)
     LUT4:I0->O            2   0.097   0.697  r2/a4/a7/Mmux_Y11 (S2_3_OBUF)
     LUT6:I0->O            1   0.097   0.279  r11/Mmux_Y41 (SUM_7_OBUF)
     OBUF:I->O                 0.000          SUM_7_OBUF (SUM<7>)
    ----------------------------------------
    Total                      3.786ns (0.486ns logic, 3.300ns route)
                                       (12.8% logic, 87.2% route)
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Fig. 6 Delay Time

VI. TABLE

Parameters	Existing CSA Design	Proposed RLPA Design
Power Consumption	0.14W	0.082W
Time Delay	5.167ns	3.786ns
Reversibility	No	Yes
Flexibility	Low	High

Table. Comparison between Existing Design and Proposed Design

VII. CONCLUSION

The difficulties of creating an effective adder for power reduction are discussed, and a reversible logic gate-based solution is shown. This discusses the numerous problems involved in creating an effective adder for power optimization and offers a solution that may be attained by utilizing reversible gates. These adders are very useful in achieving low power and high performance in many areas such as image processing applications, multimedia applications, and in hybrid applications [2,3,6,8]. The implementation of ASIC in the design has demonstrated a decrease in power usage. The internal power gained is 1.36292 nw, the overall power acquired is 12155 nw, and the leakage power of the proposed adder is 3.00411 nw. The power conservation for the adder that was designed utilizing reversible gates is about 15%. The software simulation of the proposed adder is done in Xilinx software. The hardware IC simulation may be done in the future.

VIII. REFERENCES

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