Low-Power 12T SRAM with Multi-Node Soft Error Resilence for Radiation-Hardened Applications

[1]V. Sudheer, M.Tech, [2]A. Raj Akhil, [3]K. Michael Jatin, [4]M. Prajeeth Kumar, [5]K. Abhinay, [6]G. Sai Lohith Kumar

[1]*Assistant Professor, ECE Department, N.E.C., Nellore*
[2]*UG Scholor, N.E.C., Nellore,*
[3] *G Scholor , N.E.C., Nellore,*
[4] *UG Scholor, N.E.C., Nellore,*
[5] *UG Scholor, N.E.C., Nellore,*
[6] *UG Scholor, N.E.C., Nellore*

Abstract: *The Main objective is the development of an advanced SRAM (Static Random Access Memory) design tailored for aerospace applications, where low power consumption and high reliability are critical. Traditional memory systems often face challenges related to radiation-induced upsets, particularly in high-altitude and space environments. This project introduces a novel 12T SRAM cell that incorporates dual-node upset-recovery mechanisms, enabling the system to detect and correct single-event upsets (SEUs) without significant power overhead. The proposed design significantly improves energy efficiency by reducing power consumption during both active and standby states, addressing the stringent energy constraints in aerospace systems. The System introduces a novel 12T SRAM cell, which integrates a dual-node upset recovery mechanism to mitigate the effects of radiation-induced errors, commonly encountered in high-altitude and space environments. This design ensures data integrity by enabling the system to detect and recover from single-event upsets (SEUs) without significant power overhead. The system leverages advanced radiation-hardening techniques and fault-tolerant methods, such as error correction coding (ECC) and redundancy, to enhance its resilience against radiation. In addition, the SRAM design incorporates power optimization strategies, including dynamic voltage scaling, power gating, and low-leakage transistors, to minimize energy consumption while maintaining robust performance.*

Keywords : *12T SRAM, Low Power Consumption, Radiation Hardening, Single-Event Upsets(SEUs).*

I. INTRODUCTION

The proliferation of demand for low energy devices such as wireless sensor networks, implantable medical imaging and other portable devices powered by batteries has contributed to a major design restriction for dissipation. The Static Access Memory, which occupies large proportions of Systems-on-Chip (SoCs) and its application, is the main contributor to the power dissipation.

Several combinations of SRAM cells have been suggested by the researchers to address read loss by a separate read buffer. The static range read (RSNM) of these cells is improved by decoupling the read/write route but still has a weak written margin (WM) in the sub-threshold region. In comparison, the literature documenting different writing-help

This work is licensed under a Creative Commons Attribution 4.0 International License

strategies to raise the SRAM cell compose margin. Boosting the Word-line and negative bitline (NBL) are the traditionally implemented writing assistance techniques that improve the writeability of a write access transistor by enhancing its driving power. These methods, though, contribute to region and power fines. Another effective approach to increase writability is to weaken the power of the interconnection inverter pair. It protects power cuts rises or floats, VSS cells, etc.

II. FUNCTIONAL OVERVIEW

The proposed RHBD 12T SRAM cell enhances memory reliability by addressing the susceptibility of traditional SRAM designs to single event upsets (SEUs). SEUs occur when a high-energy particle strikes a memory cell, altering its stored data. With increasing transistor density and decreasing critical charge in advanced CMOS technology, SRAMs have become more vulnerable to these reliability challenges. Conventional approaches such as triple modular redundancy (TMR) and error correction codes (ECC) provide fault tolerance but come with significant area, power, and timing overheads.

The 12T SRAM cell is designed to mitigate these challenges by incorporating additional transistors and circuit-level hardening techniques to improve fault tolerance while maintaining power efficiency and stability.

In the 12T SRAM design, the cell structure prevents data corruption by isolating storage nodes during read and write operations, reducing write disturbances.

The control signals (WLA, WLB, WL, RBL, RWL, and VVSS) ensure that critical charge distribution remains stable, and floating node issues are minimized.

The design effectively prevents data flipping, even in extreme conditions, as demonstrated through extensive 5000-cycle Monte Carlo simulations. Unlike conventional 6T and 10T cells, which struggle with multiple node upsets, the 12T cell ensures improved radiation resilience through a combination of circuit and layout-level hardening strategies.

The proposed RHBD 12T SRAM cell is particularly suited for high-radiation environments, such as aerospace applications, where reliability is paramount. Its ability to resist SEUs while maintaining low power consumption and reduced area overhead makes it a viable alternative to traditional SEU mitigation techniques.

By leveraging circuit-level enhancements, the 12T cell achieves a balance between robustness and efficiency, ensuring stable memory performance in demanding conditions.

Furthermore, its improved energy efficiency makes it an attractive choice for mission-critical applications where both power and performance are crucial.

III. METHODOLOGY

The existing SRAM systems primarily utilize 6T, 8T, and 10T cell designs, which are widely used for memory applications. These systems operate by employing cross-coupled inverters with additional access transistors for data storage and retrieval. Techniques such as voltage scaling, dual-Vt, and forward body biasing are implemented to

This work is licensed under a Creative Commons Attribution 4.0 International License

minimize power dissipation and enhance energy efficiency. However, with increasing CMOS scaling, leakage currents and process variations pose significant challenges. Traditional SRAM designs like resistive-load SRAM and depletion-load NMOS SRAM attempt to balance power consumption and stability, but their effectiveness is limited in high-density applications. Additionally, banking techniques in SRAM help reduce power consumption by selectively activating memory rows. However, they still suffer from inefficiencies related to power leakage, read stability, and access time.

Key Features of the Existing System: -

1. **6T-SRAM Topology** – Utilizes cross-coupled inverters for stable data retention.
2. **Banked Organization** – Reduces switching power by activating only specific memory sections.
3. **Forward Body Biasing** – Lowers sub-threshold leakage currents.
4. **High-K Gate Dielectrics** – Minimizes gate leakage current for power efficiency.
5. **Multiple Transistor Configurations** – Uses resistive-load, depletion-load, and CMOS-based SRAM cells.

Disadvantages of the Existing System: -.

1. **High Leakage Power** – Increasing transistor density leads to excessive power dissipation.
2. **Process Variations** – Scaling below 100nm makes SRAM cells more susceptible to reliability issues.
3. **Lower Noise Margins** – Voltage scaling decreases the signal swing, impacting stability.
4. **Increased Complexity** – Techniques like dual-Vt and forward body biasing add circuit complexity.
5. **Higher Read/Write Delays** – Additional circuit techniques and transistor configurations can slow down access times.

PROPOSED SYSTEM

The proposed system introduces a radiation-hardened by design (RHBD) 12T SRAM cell to enhance memory reliability in harsh environments, particularly for aerospace applications. Unlike conventional SRAM cells that are susceptible to single event upsets (SEUs) caused by radiation exposure, the proposed 12T cell incorporates circuit-level hardening techniques to mitigate multiple-node disruptions. It achieves this by isolating storage nodes from disturbance pathways, preventing write disturbance, and ensuring improved stability compared to existing designs such as the 6T, 10T, and 13T SRAM cells. The 12T cell also reduces static power dissipation during standby mode, making it an energy-efficient alternative.

This work is licensed under a Creative Commons Attribution 4.0 International License

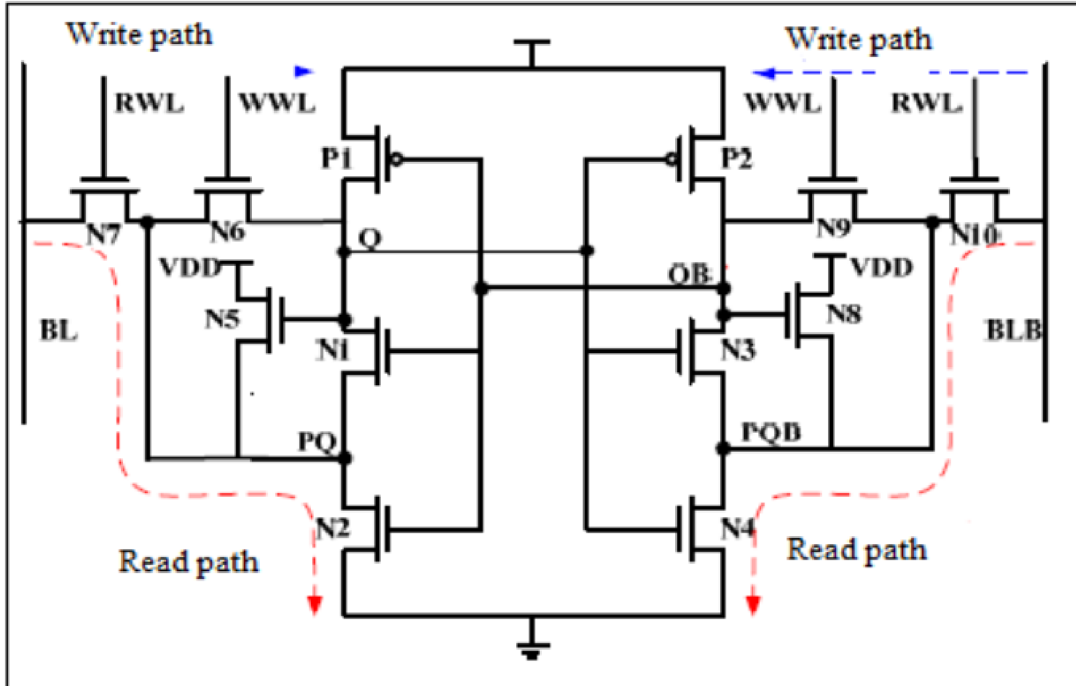

Fig.3.1: Proposed 12T SRAM cell.

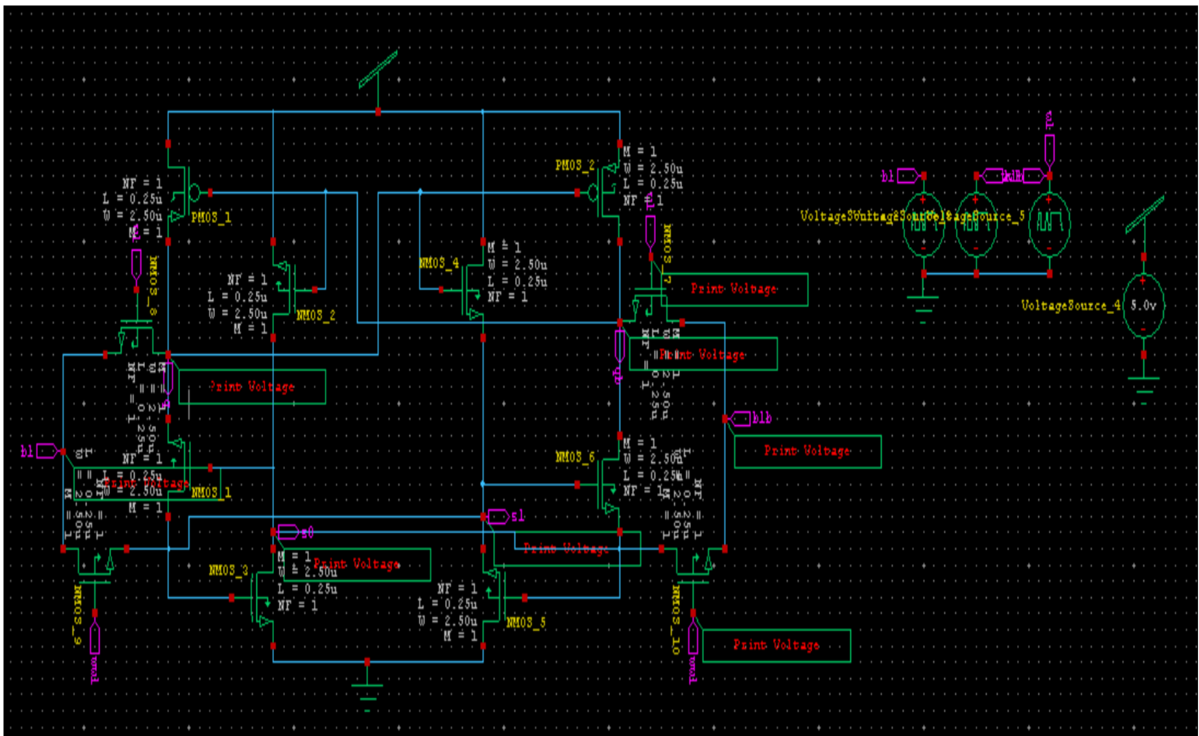

Fig.3.2: Schematic of Proposed 12T SRAM cell.

This work is licensed under a Creative Commons Attribution 4.0 International License

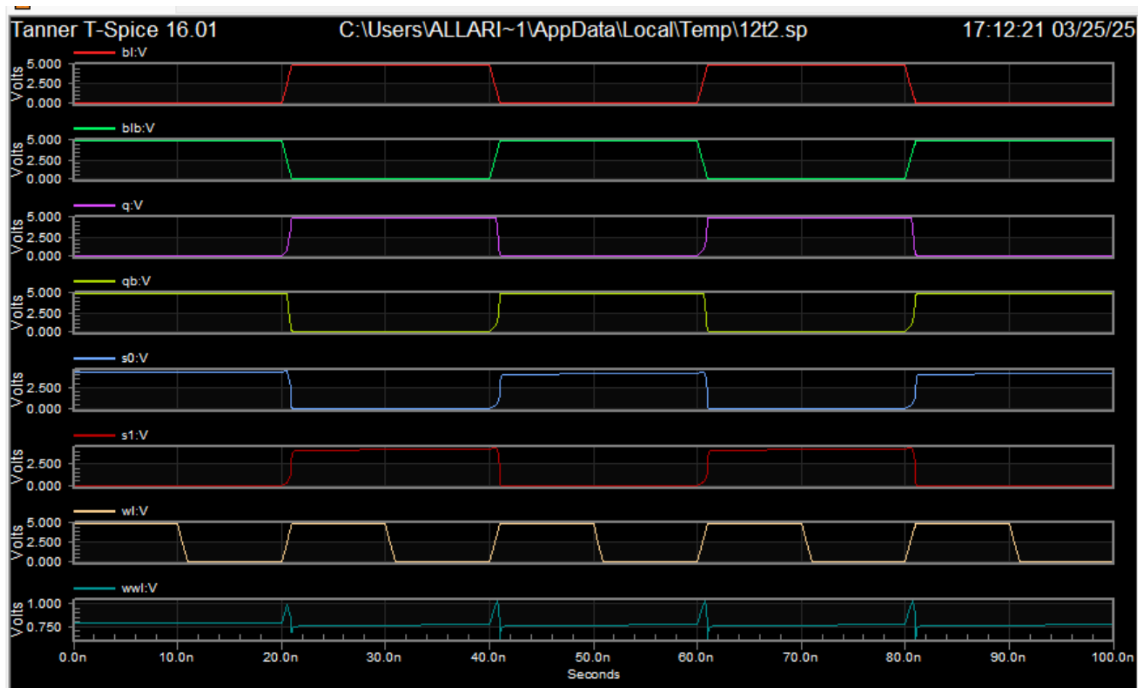

Fig.3.3: Simulation Result of Proposed 12T SRAM cell.

Features : -

1. **Improved SEU Resilience** – The 12T cell structure minimizes susceptibility to single-event upsets by isolating the storage node from unwanted disturbances.
2. **Enhanced Stability** – Unlike the existing 6T and 10T cells, the proposed design prevents unintended data flips and floating node issues, ensuring data integrity.
3. **Lower Power Consumption** – By using selective transistor activation, the system significantly reduces static power dissipation, overcoming the high leakage issue in existing designs.
4. **Reduced Area Overhead** – Compared to TMR-based approaches, the 12T design achieves higher fault tolerance with fewer transistors, optimizing space utilization.
5. **Minimal Delay Impact** – Unlike ECC-based approaches that introduce high processing delays, the proposed 12T cell maintains fast read/write access times, improving real-time memory performance.

IV. COMPONENTS

SOFTWARE COMPONENTS

1. Software Tools:

Tanner EDA provides a suite of tools essential for VLSI design and simulation. The main tools required are:

- **S-Edit** – A schematic entry tool used to design and document circuits before simulation and layout design.
- **T-SPICE** – A SPICE-based simulation engine that performs circuit analysis and validation.
- **W-Edit** – A waveform viewer used to analyze simulation results and verify circuit performance.
- **L-Edit** – A physical design tool for chip layout and design rule checks (DRC).

This work is licensed under a Creative Commons Attribution 4.0 International License

2. Libraries & SPICE Models:

- **Tanner_Libraries.zip** – Contains basic circuit elements such as resistors, capacitors, NMOS, and PMOS transistors.
- **Generic_025 SPICE Models** – Provides technology-specific models for MOSFET transistors used in CMOS circuit design.

3. Hardware Components (if required for practical implementation):

- **Personal Computer (PC)** – Required for running Tanner EDA software and performing simulations.
- **Integrated Circuit (IC) Fabrication Kit** – Used for physical testing of designed circuits.
- **Power Supply & Signal Generators** – For verifying circuit functionality in real-world conditions.

V. CONCLUSION

The suggested memory cell's key contribution is its ability to effectively guard against multiple-node upsets, in addition to its tolerance for single-node upsets. The SEU resilience of the process is further confirmed by 1000 MC simulations, the results of which show that process change has no effect on the robustness of the SEU.

One possible drawback to the proposed 12T memory cell is that it has a longer read access time than current memory technologies, which might slow down some high-speed applications. However, memory size, resilience, and dependability may be more significant in mission-critical aircraft applications. Therefore, the RHBD 12T memory cell suggested in this study is a good design for radiation robustness in comparison to other state-of-the-art hardened memory cells, as seen from the perspective of a critical application designer. As a result, the general approach to improving this to focus on minimising its space overhead while simultaneously increasing its time performance.

Since the BTI causes a change in the transistor's Vth value, it is one of the most difficult reliability issues to solve at the Nano scale.

Degradation of SNM occurs due to a Vth shift in the transistors of SRAMs. In this study, Presents a sensor that can detect BTI deterioration in SRAM cells reliably so that their ageing can be tracked. To this end, it is necessary to monitor the peak of IV_{dd}/IGnd of the SRAM block during the write operation to get a sense of the NBTI/PBTI-aging of the SRAM cells.

The CCVS measures this current and produces an equivalent voltage. The frequency of the VCO's oscillations is determined by the peak of this voltage. The magnitude of the BTI effect may be seen in the frequency shift of the oscillations relative to the reference frequency of a freshly synthesised cell. The BTI

This work is licensed under a Creative Commons Attribution 4.0 International License

status of any given row or even individual cells may be determined by reading the values stored in the SRAM.

Advancements in RHBD

- Further optimization of RHBD (Radiation-Hardened by Design) memory cells with improved fault tolerance for extreme environments like space and nuclear applications.
- Exploration of new materials and 3D-stacked architectures to enhance radiation resilience.

Scaling and Power Efficiency Improvements

- Development of ultra-low-power SRAM designs with reduced leakage for energy-efficient IoT and AI applications.
- Use of emerging nanotechnologies like FinFET, TFET, and CNTFET to improve performance and minimize power dissipation.

Artificial Intelligence & Machine Learning Applications

- Implementing AI-driven error detection and correction techniques to enhance SRAM reliability in high-radiation environments.
- Utilizing machine learning models to predict aging effects like Bias Temperature Instability (BTI) and optimize memory performance over time.

Integration with Quantum and Neuromorphic Computing

- Investigating hybrid memory architectures combining classical CMOS-based SRAM with quantum computing elements for next-gen processors.
- Adapting SRAM designs for neuromorphic computing systems, improving AI-driven data storage and retrieval.

Security Enhancements

- Development of SRAM-based cryptographic methods for secure data storage in defense and aerospace applications.
- Implementing physically unclonable functions (PUFs) using SRAM variations for enhanced cybersecurity.

VI REFERENCES

[1] Akshatha P Inamdar ; P A Divya ; H. V. Ravish Aradhya “Single bit-line low power 9T static random access memory”, 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT) Electronic ISBN: 978-1-5090-3704-9.

This work is licensed under a Creative Commons Attribution 4.0 International License

[2] Uddalak Bhattachara et al.,2008 "45nm SRAM Technology Development and Technology Lead Vehicle" Intel Technology Journal, Volume 12, Issue 2 .

[3] Milad Zamani, Sina Hassanzadeh, Khosrow Hajsadeghi and Roghayeh Saeidi, 2013"A 32kb 90nm 9T -cell Subthreshold SRAM with Improved Read and Write SNM" 8th International Conference on Design and Technology of Integrated Systems in Nanoscale Era(DTIS).

[4] Arvind Chakrapani 2018, "Survey on the design methods of low power SRAM cell" in International Journal of Pure and Applied Mathematics.

[5] Singh Jawar, Mathew Jimson, Pradhan Dhiraj K., Mohanty Saraju P. 2008 "Failure analysis for ultra low power nano-CMOS SRAM under process variations". Soc Conference, IEEE international, IEEE conference publications, P251 -254.

This work is licensed under a Creative Commons Attribution 4.0 International License