DESIGN OF AN OPTIMIZED 4-BIT RIPPLE CARRY ADDER USING AN EXACT REVERSIBLE FULL ADDER

[1]A. Siva Sai Kumar [2]P. Sahithi [3]B. Radhika [4]L. Vyshnavi [5]R. Dharani[6]E. Sujana

[1]Assistant Professor, ECE Department, N.E.C., Nellore
[2]Assistant Professor, ECE Department, N.E.C., Nellore
[3] UG Scholor, N.E.C., Nellore,
[4] UG Scholor, N.E.C., Nellore,
[5] UG Scholor N.E.C., Nellore,
[6] UG Scholor, N.E.C., Nellore,

Abstract: *The advent of quantum computing and low-power applications has highlighted the significance of reversible logic in designing energy-efficient circuits. In this work, I propose the design and implementation of a 4-bit ripple carry adder (RCA) using the newly introduced Exact Reversible Full Adder (ERFA), which demonstrates a quantum cost (QC) of 9 and a total delay of 7Δ. The ERFA, constructed using 4 Feynman gates and 1 Fredkin gate across three stages, features 2 ancillary inputs (AIs) and 3 garbage outputs (GOs). Leveraging this novel adder, I extend its functionality to build a 4-bit RCA by cascading four ERFAs. The proposed 4-bit RCA is verified through functional simulations using Verilog HDL. Further, the design metrics of the proposed 4-bit RCA are evaluated and compared with existing reversible RCA designs in terms of quantum cost, delay, and gate efficiency. The results demonstrate the advantages of our design in achieving lower quantum cost and efficient gate utilization, making it suitable for quantum and reversible computing applications.*

I. INTRODUCTION

In recent years, the demand for energy-efficient and quantum-compatible computing systems has grown significantly due to advancements in quantum computing and low-power applications. Reversible logic has emerged as a promising solution for designing such systems, as it minimizes energy dissipation by preventing information loss, in line with Landauer's principle.Arithmetic circuits, particularly adders, form the backbone of many computational systems. However, existing designs for reversible ripple carry adders (RCAs) often exhibit high quantum cost, increased delay, and inefficient utilization of logic gates, limiting their suitability for advanced applications.

This project focuses on the design and implementation of a 4-bit ripple carry adder (RCA) using a newly introduced Exact Reversible Full Adder (ERFA). The ERFA is optimized for low quantum cost and delay, utilizing 4 Feynman gates and 1 Fredkin gate in a three-stage configuration. The design features 2 ancillary inputs and 3 garbage outputs, achieving a quantum cost of 9 and a delay of 7Δ. By cascading four ERFAs, construct a 4-bit RCA and evaluate its performance through functional simulations using Verilog HDL.

II. FUNCTIONAL OVERVIEW

The project titled **"Design of an Optimized 4-bit Ripple Carry Adder Using an Exact Reversible Full Adder"** focuses on optimizing the design of a 4-bit ripple carry adder (RCA) circuit by incorporating an exact reversible full adder (FA) in the design. To understand the functionality of this project, let's break it down into key components and objectives:

1. Ripple Carry Adder (RCA) :

- **RCA** is a simple digital circuit used for adding two binary numbers. It works by adding the bits of the numbers sequentially, starting from the least significant bit (LSB) and propagating the carry bit to the next higher bit position.
- In an RCA, each stage consists of a full adder (FA), which computes the sum of the corresponding bits and a carry bit from the previous stage.
- The primary disadvantage of an RCA is its relatively slow speed, as the carry bit has to propagate through each adder stage, resulting in a delay that increases with the number of bits.

2. Full Adder (FA):

- A **full adder** is a fundamental building block in digital electronics. It adds three input bits (two data bits and a carry-in) and generates a sum and carry-out.
- The exact reversible full adder used in this design is optimized for energy efficiency and minimal power dissipation. It is also **reversible**, meaning that it has the property that both inputs and outputs can be recovered from the output. This is important for minimizing energy loss due to heat dissipation, making the design more energy-efficient.

3. Reversible Logic:

- **Reversible logic** refers to circuits that can operate without dissipating energy, following Landauer's principle, which states that irreversible logic leads to energy loss. Reversible circuits can theoretically perform computations without generating heat, which makes them ideal for low-power applications.
- In this project, by using reversible logic in the full adder, the design aims to optimize power consumption while maintaining the functionality of a traditional adder.

4. Optimized 4-bit RCA with Reversible FAs:

- The project involves creating an optimized 4-bit **Ripple Carry Adder** that uses reversible full adders. By implementing reversible logic in the full adders, the overall power consumption and heat dissipation are reduced.
- The optimization could include improvements in the gate-level design of the adder to reduce delays, minimize power usage, or increase overall speed without compromising functionality.
- **Optimization goals** might involve:
    - **Power efficiency**: Minimizing the energy consumed during the computation.
    - **Delay reduction**: Improving the speed of the adder by optimizing the carry propagation.
    - **Area efficiency**: Minimizing the size of the circuit.

5. Key Objectives of the Project:

- **Design and simulation** of a 4-bit ripple carry adder using exact reversible full adders.
- **Optimization of power consumption** through the use of reversible logic, which is expected to lead to energy-efficient designs suitable for low-power applications.

- **Performance comparison**: Evaluating the performance of the optimized design against traditional RCA circuits in terms of power, delay, and area.

6. Benefits of the Reversible Full Adder:

- **Low Power Consumption**: Since the reversible full adder doesn't generate unnecessary heat, the overall adder circuit will be more power-efficient.
- **Energy Efficiency**: This can result in an adder that is more suitable for portable or battery-operated devices where power consumption is critical.
- **Reversibility**: By using reversible logic, the circuit becomes more energy-efficient, which could be important in advanced computing systems where energy conservation is a priority.

7. Applications:

- **Low Power Digital Systems**: Useful in battery-powered and portable devices.
- **Quantum Computing**: Reversible circuits are fundamental in the development of quantum computing, where energy efficiency is crucial.
- **Embedded Systems**: Used in embedded processors and microcontrollers where power consumption is a key concern.

8. Implementation:

- The project will likely involve the use of **hardware description languages (HDLs)** like VHDL or Verilog to model the circuit.
- **Simulation tools** (e.g., Xilinx, Cadence, or ModelSim) will be used to verify the correctness and performance of the design.
- The design would be optimized for **low-power, high-performance operation** while maintaining the simplicity of the original 4-bit ripple carry adder.

9. Expected Outcomes:

- A fully functional 4-bit ripple carry adder with optimized performance in terms of power consumption, speed, and area, using reversible logic gates for the full adders.
- A comparison of the optimized adder's performance with that of traditional RCA designs

III. METHODOLOGY

EXISTING SYSTEM

The Existing System has High Quantum Cost (QC) and Delay which is considered as the one of the major disadvantage.

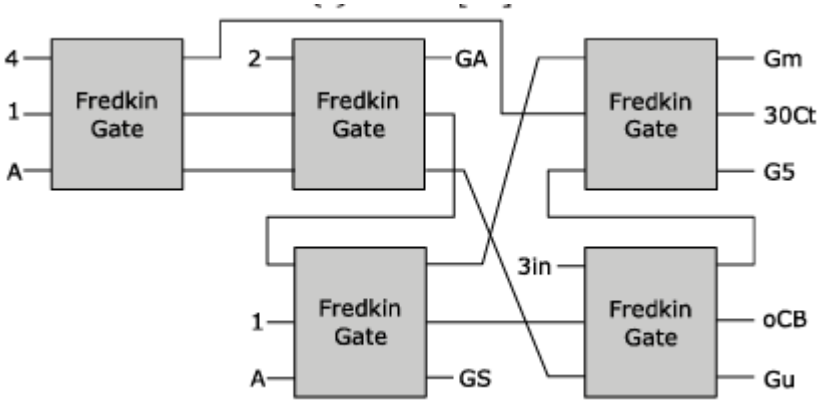

Fig3.1 Block Diagram of an Existing System

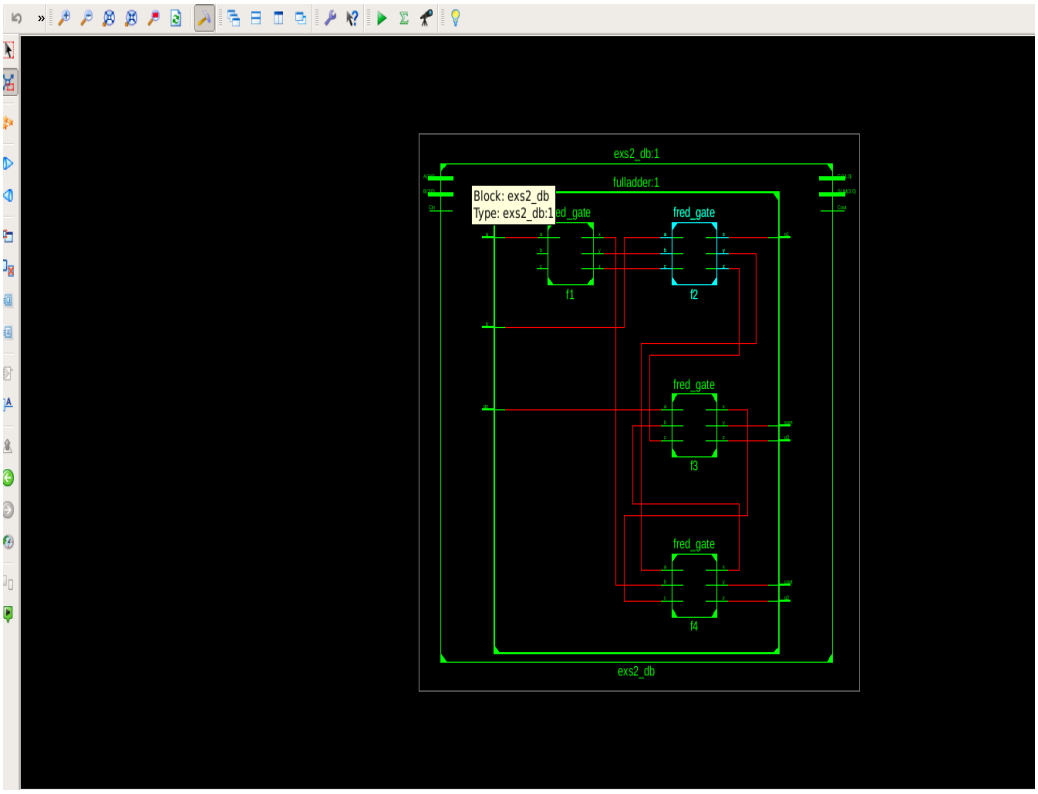

Fig3.2: RTL Schematic of Existing System

To overcome the Disadvantage we have created a Block Diagram with minimum Quantum Cost and Minimum Delay as shown below.

PROPOSED SYSTEM

In this paper, present a new exact reversible full adder has a 'quantum cost' (QC) of 9 with total delay of 7Δ. The proposed adder herein referred to as "Exact Reversible Full Adder" (ERFA). The proposed ERFA is designed using 4- Feynman gates and 1Fredkin gate in three different stages. The proposed ERFA has '2' ancillary inputs (AIs) and '3' garbage outputs (GOs). Further, to verify the functionality, the proposed ERFA is designed and validated through Verilog HDL code simulation. Also, it is compared in terms of various design metrics (DMs) against 16 reversible full adders that were reported in the current literature.

Exact Reversible Full Adder (ERFA) Design

This design introduces an **Exact Reversible Full Adder (ERFA)**, which is optimized for **low quantum cost (QC)**, **minimal delay**, and **efficient gate utilization** while maintaining reversibility.

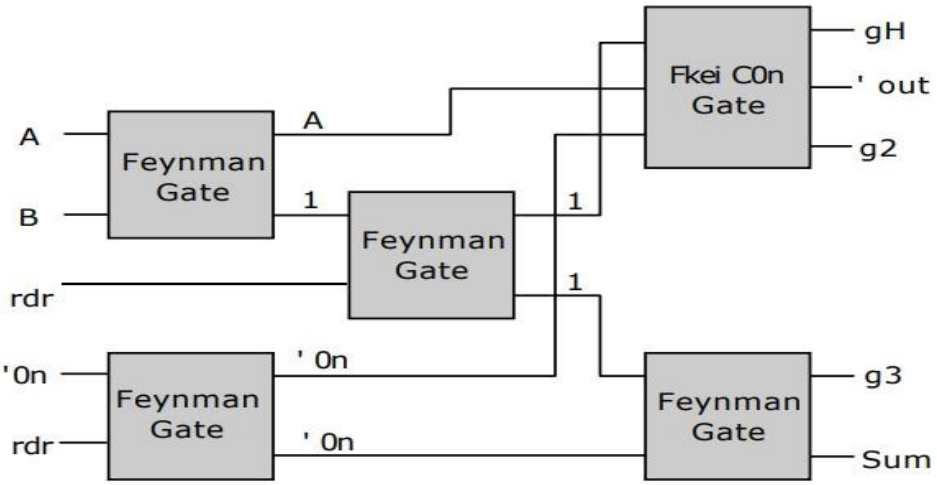

Fig3.3: ERFA Block Diagram

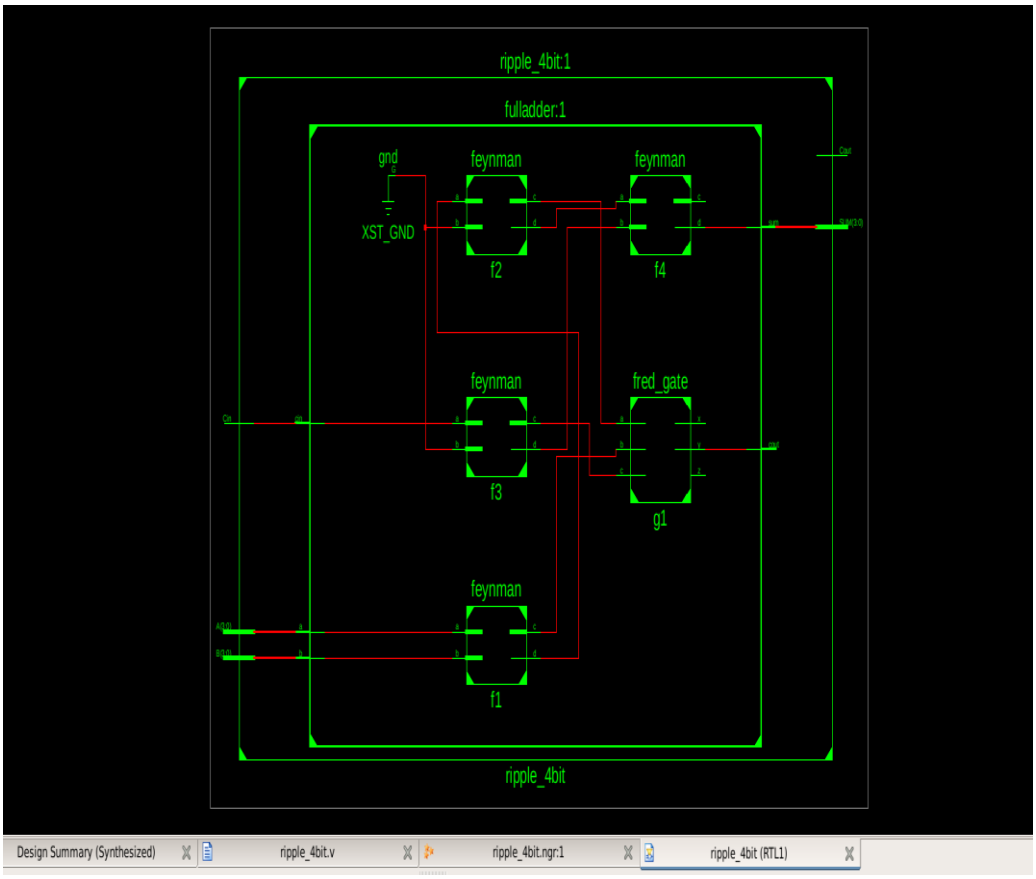

Fig3.4: RTL Schematic of Proposed System

COMPARISION: EXISTING VS PROPOSED

Table shows the difference between the existing and proposed systems of the 4-Bit Ripple carry adder.

PARAMETERS	EXISTING SYSTEM	PROPOSED SYSTEM
AUXILIARY INPUTS	2	2
GATE OUTPUTS	3	3
QUANTUM COST	20	9
DELAY	20	7

Table 3.1: Existing vs Proposed

The proposed system maintains the same input and output requirements while significantly improving performance by reducing quantum cost and delay. These optimizations indicate that the new system is more efficient, resource-friendly, and faster, making it a preferable alternative to the existing system.

IV.SOFTWARE DESCRIPTION

XILINX ISE

Xilinx Tools is a suite of software tools used for the design of digital circuits implemented using Xilinx Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD). The design procedure consists of (a) design entry, (b) synthesis and implementation of the design, (c) functional simulation and (d) testing and verification. Digital designs can be entered in various ways using the above CAD tools: using a schematic entry tool, using a hardware description language (HDL) – Verilog or VHDL or a combination of both. In this lab will only use the design flow that involves the use of Verilog HDL.

The CAD tools enable to design combinational and sequential circuits starting with Verilog HDL design specifications. The steps of this design procedure are listed below:

1. Create Verilog design input file(s) using template driven editor.
2. Compile and implement the Verilog design file(s).
3. Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA or CPLD).

4. Assign input/output pins to implement the design on a target device.

5. Download bitstream to an FPGA or CPLD device.

6. Test design on FPGA/CPLD device

A Verilog input file in the Xilinx software environment consists of the following segments:

Header: module name, list of input and output ports.

Declarations: input and output ports, registers and wires.

Logic Descriptions: equations, state machines and logic functions.

End: endmodule

V.RESULTS

EXISTING SYSTEM

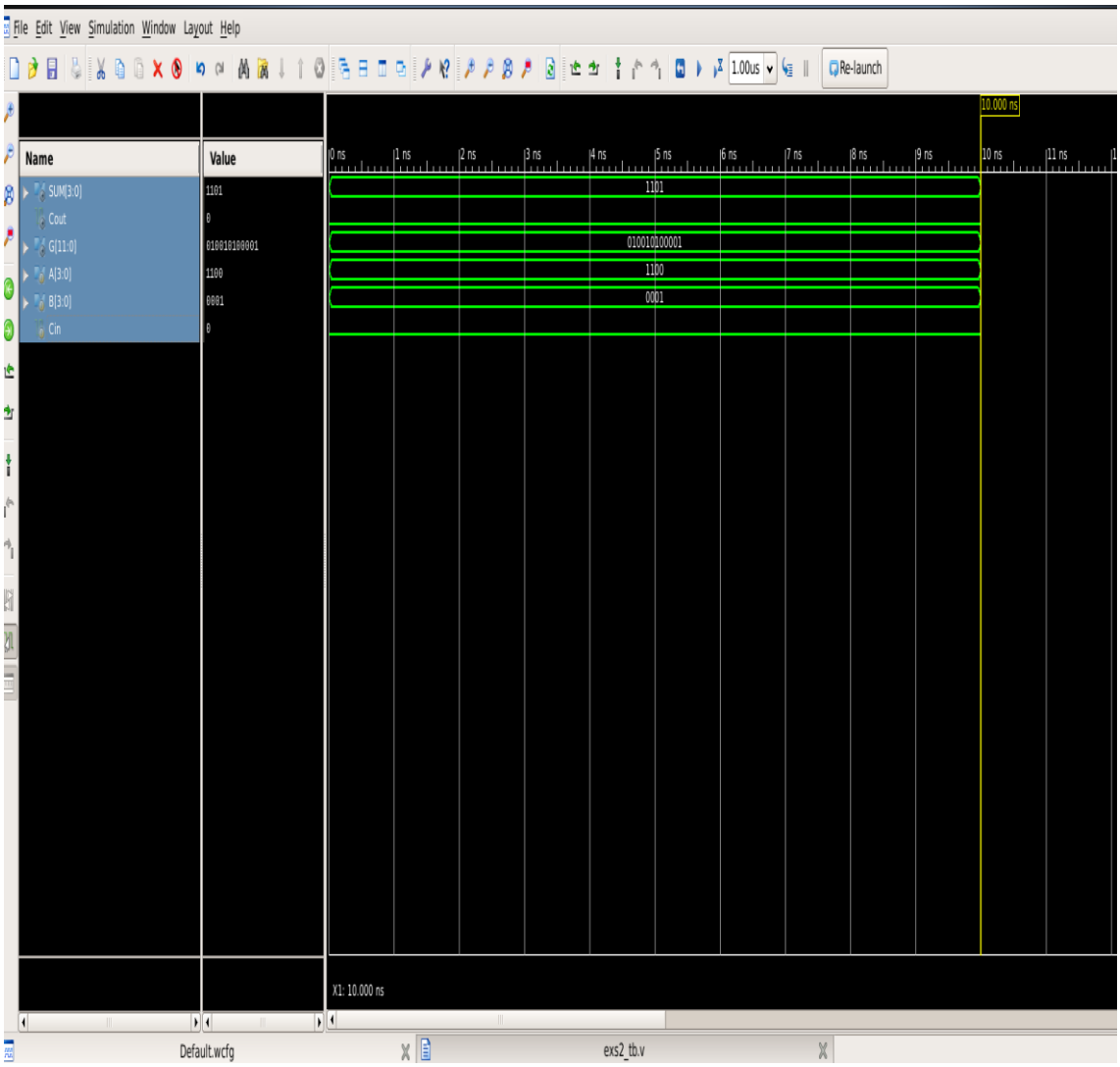

Fig 5.1: Output Waveform of an Existing system

PROPOSED SYSTEM

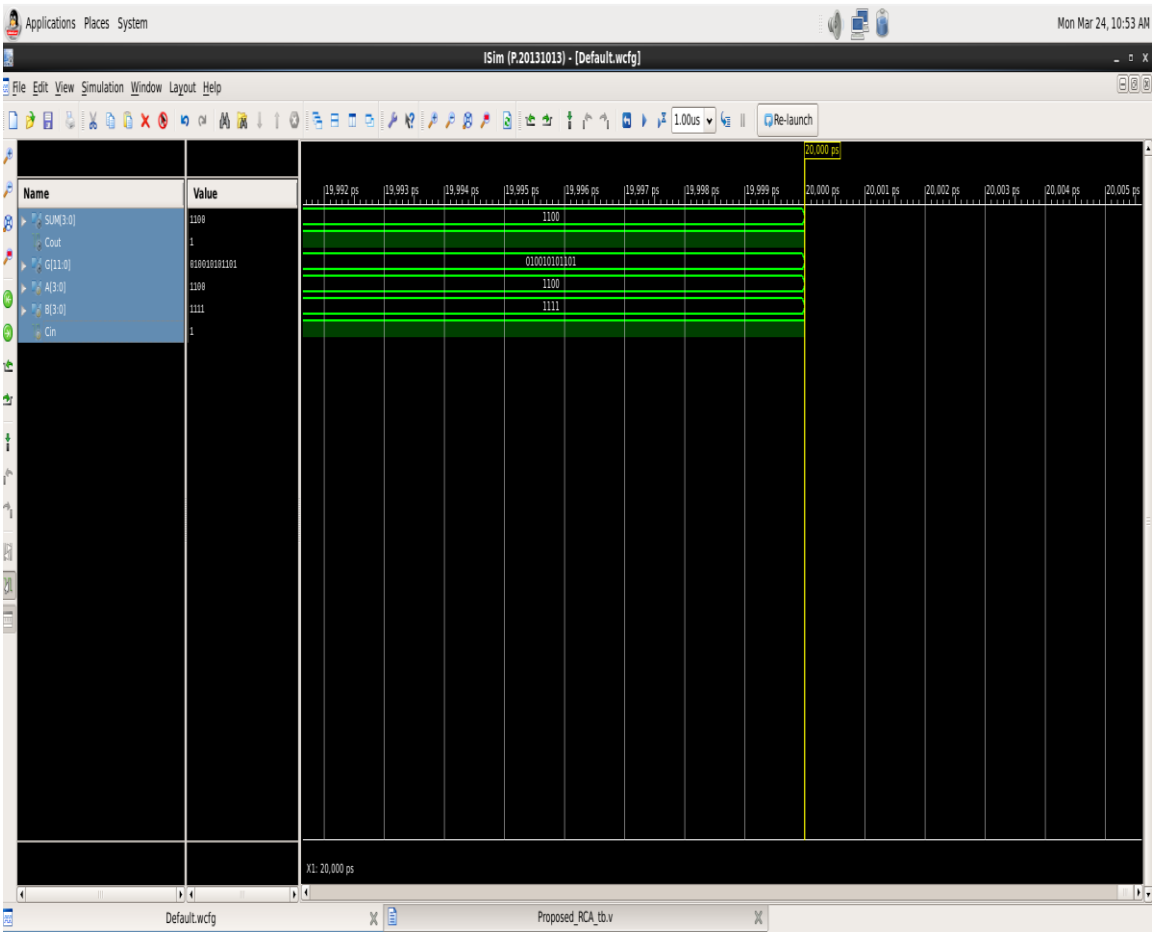

Fig 5.2: Output Waveform of a Proposed system

VI.CONCLUSION & FUTURE SCOPE

CONCLUSION

The design of the 4-bit Ripple Carry Adder (RCA) using the proposed Exact Reversible Full Adder (ERFA) achieves efficient computation with reduced quantum cost, delay, and resource utilization. By incorporating Feynman and Fredkin gates, the ERFA-based RCA ensures reversibility while minimizing ancillary inputs and garbage outputs. The proposed approach enhances the performance of traditional ripple carry adders by optimizing logical operations and maintaining low power dissipation, making it suitable for quantum and low-power computing applications.

Overall, the implementation of the 4-bit RCA demonstrates the effectiveness of reversible logic in arithmetic circuits. The proposed design provides a scalable and efficient solution for multibit addition while preserving quantum computing principles. This work contributes to the advancement of reversible computing,

offering a foundation for future improvements in arithmetic unit designs for quantum processors and energy-efficient digital systems.

FUTURE SCOPE

- Expanding the design to multi-bit and multi-operand reversible arithmetic units.
- Implementing the ERFA in practical quantum processors for error-free quantum computations.
- Integrating machine learning techniques for optimizing reversible circuit designs.
- Extending research to develop reversible multipliers and ALUs for complete low-power computing architectures.

The future scope of this project extends across multiple domains, including VLSI, quantum computing, AI, and IoT. The proposed Exact Reversible Full Adder (ERFA) can be expanded to multi-bit arithmetic units, such as reversible subtractors, multipliers, and complete arithmetic logic units (ALUs), enabling more complex and efficient computations. With the rapid advancements in quantum computing, the ERFA can be adapted for quantum arithmetic circuits, improving computational efficiency and minimizing power loss. Its low-power characteristics make it ideal for integration into energy-efficient processors, AI accelerators, cryptographic hardware, and edge computing systems.

Future developments may also explore emerging technologies like nanotechnology, memristors, and optical computing to further optimize performance. The ERFA can play a vital role in machine learning and AI-driven applications, particularly in neural network accelerators requiring low-energy arithmetic operations. Additionally, its potential in IoT, biomedical electronics, and wearable devices makes it a key component in ultra-low-power embedded systems. As reversible computing gains prominence, this project could contribute to industry standards and research in designing reversible circuits, paving the way for next-generation sustainable and high-performance computing architectures.

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